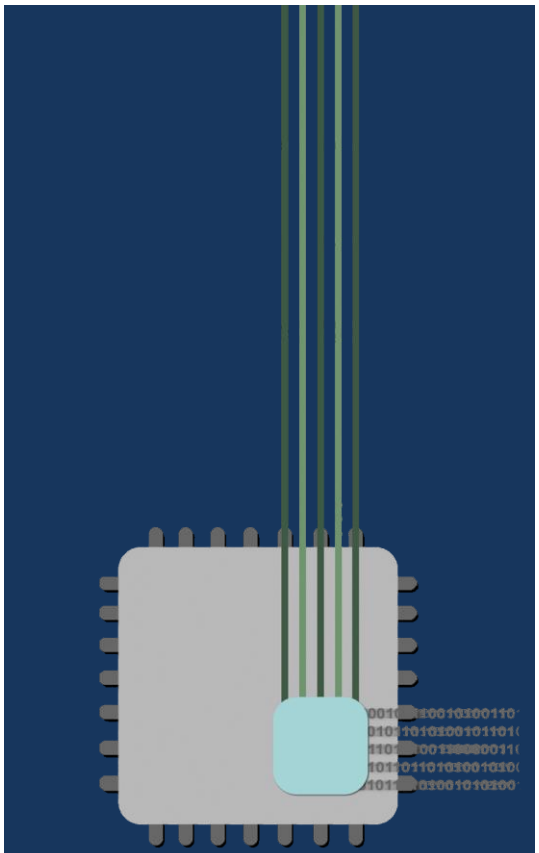
DO-254 Certifiable ARINC 429 IP Core for FPGAs

ARINC429IP

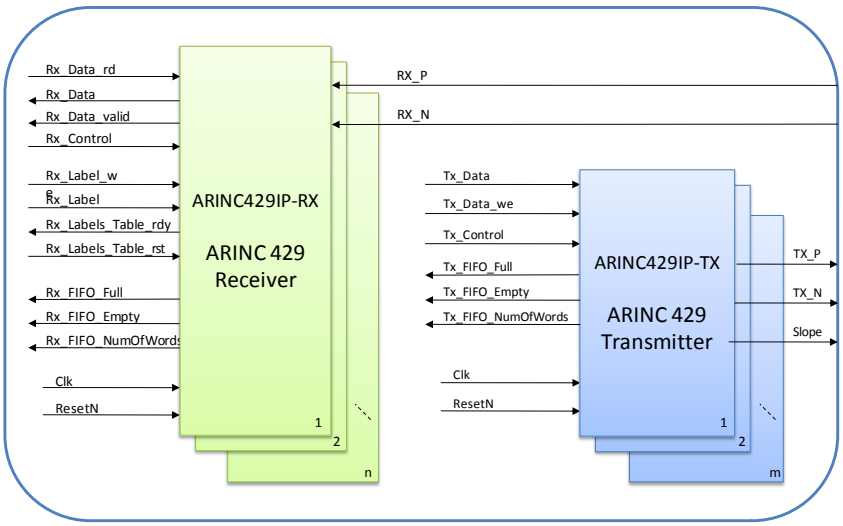
ARINC 429 IP Core with modular transmitters and receivers Certifiable for DO-254 DAL-A

Compact, Robust, Reliable
MIL-STD-IP-Cores



Key Features and Benefits

- ARINC 429 specification compatible
- Separated channels for ARINC 429 Data Transmit and Receive
- 32 bits wide, programmable depth, separated FIFO buffers for transmit and receive
- Includes noise filtering mechanism to enhance receiver robustness
- Programmable data rate on each channel (12.5/100 Kbps)
- Programmable label recognition with 256 Labels for each Receiver
- Programmable parity: Even, Odd or No-parity (32nd bit as data)
- FIFO full/empty indication
- Supports standard ARINC 429 line drivers/receivers with two bits data and slope bit controls
- Multiple running clock options to reduce design time domains
- Small FPGA area utilization
- Modular architecture allowing flexible implementations. Any number of transmitters and receivers available in a single Netlist.
- Provided with full verification environment
- Based on vendor and technology independent VHDL code
- Provided with documentation to certify the design for DO-254 DAL-A



Designed from ground up for use in aerospace, avionics and military, Sital's IP products, offer uniquely compact, robust and reliable solutions for any PLD/FPGA and ASIC device.

More products from Sital:

- *MIL-STD-1553 IP Core, DDC® compatible with local bus interface*
- *MIL-STD-1553 IP Cores for simple BC/RT/MT Applications.*
- *MIL-STD-1553 Discrete Components Transceiver*
- *MIL-STD-1553 Testers.*
- *MIL-STD-1553 Design Services*
- *ARINC 429 IP Core*
- *PCI IP core*

More information available at **www.sitaltech.com**

SITAL Technology

ARINC429IP

Supported FPGAs

- Any FPGA with sufficient number of LUTs and Dual-Port memory
- FPGA families from the following vendors:
  - Xilinx
  - Altera
  - Lattice
  - Actel

** For other FPGAs or ASIC please consult Sital*

ARINC429IP Deliverables

- EDIF net list for the desired FPGA family, core configuration, clock frequency and FIFO depth
- User's manual
- Sample VHDL code that incorporates the core
- Synthesis script for sample code
- DO-254 certification documentation (upon request)

Available Configurations

- **ARINC429IP-TX**: ARINC 429 transmitter
- **ARINC429IP-RX:** ARINC 429 receiver
- **ARINC429IP-RX-n-TX-m:** ARINC429, 'n' receivers and 'm' transmitters

ARINC 429 Tx/Rx Core Operation

The ARINC429IP Core is divided between two independent modules for transmit (ARINC429IP-TX) and receive (ARINC429IP-RX).
A user can order any combination of transmitters and receivers which are packaged under the same FPGA netlist.
Each ARINC 429 channel (Rx / Tx) has 32 bits wide FIFO memory. (FIFO depth is selectable by the user).

ARINC 429 Transmitter

Whenever a data is written into to the Tx_FIFO, the **ARINC429IP-TX** Core will start transmitting this data to the serial Tx ports based on the Tx channel control register configuration. Data will be transmitted consequentially word after word until the Tx_FIFO will become empty.
Tx_FIFO status (Empty/Full) and Number_Of_Words are reported in the dedicated ports.
Once FIFO_Full is asserted, there is no option to write new words to the Tx_FIFO.

ARINC 429 Receiver

The **ARINC429IP-RX** Core receives data from the ARINC 429 bus and converts it to the local bus. This core performs serial-to-parallel conversion, gap/parity check as well as baud-rate and pulse-width validation on the received data.
A noise filtering mechanism is implemented to enhance the receiver robustness and improve bit decoding. The received ARINC 32-bit word is checked for correct decoding and label matching (based on the Control Register). Invalid ARINC words or words which do not meet the necessary matching are ignored and are not loaded into the FIFO.
Each ARINC429IP-RX core contains a Programmable Labels Table which stores up to 256 labels for label recognition. If label-compare is enabled (in the control register), the Rx Core will store in its FIFO only words which passed label matching to the labels in the Table.
Specific control lines are used to reset and program labels in the Labels Table.

Advanced Verification

To ensure a fully reliable and robust product the core was developed using an advanced verification environment that includes a Random-Generation engine, Code-Coverage and assertion tools.
All ARINC429 functions and performance requirements were verified.

DO-254 Certification

The ARINC429IP IP Core can be certified with DO-254 DAL-A through DAL-E.
Along with the IP, Sital provides a testing environment and a set of documents, which the user is required to present to the certification authorities.

Simple Integration

In order to simplify the integration of the core, a sample VHDL design that uses the core is provided, including:

- A comprehensive user's manual.
- A VHDL gate level model of the core for the target technology.
- A Transceiver VHDL model that connects the core with 2 buses.
- A bus tester VHDL model that generates ARINC 429 messages and checks the return replies.
- A top Test bench that instantiates all of the components to a working example.
- A simulation script for compiling and running the core.

About Sital Technology

Founded in 1993, Sital Technology is a leading provider of IP cores and products for Mil-Std-1553, ARINC 429 and Can bus.

SITAL Technology's key quality resource is its creative, talented and professional staff. Our engineers are veterans of the Israeli Air Force, who served in the technical units of the F-16 avionics systems. They gained knowledge and experience with the MIL-STD-1553 standard from the bottom up, both as design engineers for MIL-STD-1553 components and as technicians working on the aircrafts.

Among our many customers you can find NASA, Israeli Aircraft Industries (IAI), Rafael, Elbit, Astronautics, Tadiran, Israeli Ministry of Defense, Elta, Honeywell, BAE Systems, RADA and many others.

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