



Total-EBR1553SPI

April 2024

Description

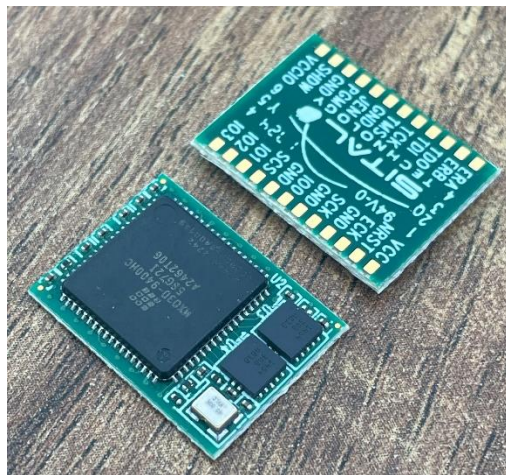
The Total-EBR1553SPI is the first fully integrated EBR-1553 solution that incorporates the host interface, MIL-STD-1553 notice 2 engine, and physical layer RS485 transceiver, in a compact 12.6mm X 17 mm QFN package.

The Total-EBR1553SPI is based on the same MIL-STD-1553B engine that drives all of Sital technology's solutions since 2005, and enjoys the quality and reliability levels that Sital Technology has set since then.

EBR-1553 was never standardized properly and thus suffer from having several dialects and challenges that these components solve. Please refer to the **Challenges with EBR1553 interface** section below.

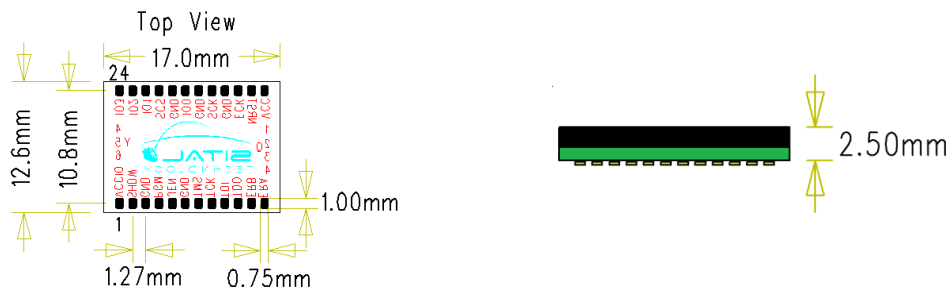
Features:

- Complete SPI to EBR-1553 component.
- MIL-STD-1553B engine migrated from legacy 1Mhz.
- EBR-1553 with DDC© Enhanced Mini Ace (EMA©) compatible register-memory map and setup.
- Supports existing DDC© EMA© software, with minimal to no change.
- Supports BC or RT or MT or RT MON modes of operation with single RS485 line.
- Supports up to 16K x 16 memory.
- Internally operates at 80 Mhz.
- Defaults to EBR-1553 industry standard Link mode.
- SPI and Dual SPI slave interface, up to 50 Mhz SPI Clock.
- Automatic detection of Single SPI or Dual SPI, no control needed.
- SPI burst of any length for highest efficiency of host interface.
- SPI signaling in Mode 0: data is sampled on the rising edge of the clock pulse and shifted out on the falling edge of the clock pulse.
- Software Libraries and Drivers available for Windows®, Peta Linux, Bare Metal & VxWorks®
- Fabricated In USA.





PIN Name	Pin NO.	TYPE	Description
VCCIO	1	IO POWER	Supply for DIGITAL IO signals. Set to 3v3. Can support 1v8 or 2v5.
INTn	2	DIGITAL IO	Hardware Interrupt output, active low.
GND	3	POWER	GROUND
N/C	4	N/C	Please provide PCB access to this pad.
JTAG_EN	5	JTAG	JTAG Enable, active high. JTAG is accessible when this signal is high. Leave low for normal operation.
GND	6	POWER	GROUND
TMS	7	JTAG in	Test Mode Select input pin. Used for Device firmware update.
TCK	8	JTAG in	Test Clock input pin. Used for Device firmware update.
TDI	9	JTAG in	Test Data input pin. Used for Device firmware update.
TDO	10	JTAG out	Used for Device firmware update.
EBRA	11	Bus input/output	EBR-1553 bus pin. Non-inverting driver output and receiver input
EBRB	12	Bus input/output	EBR-1553 bus pin. Inverting driver output and receiver input
VCC	13	POWER	3v3 supply. 130 mA maximum.
ResetN	14	DIGITAL IO	Device Reset input. Active low
Spare	15	Spare DIGITAL IO	Provide means to connect to this pin for future upgrade.
GND	16	POWER	GROUND
SPI_CLK	17	DIGITAL IN	SPI Clock In. Up to 50 Mhz.
GND	18	POWER	GROUND
SPI_MOSI SPI_IO0	19	DIGITAL IO	Single SPI Mode: Master to Slave input to Total-EBR1553SPI. Dual SPI Mode: Input or Output data, even bits to Total-EBR1553SPI.
GND	20	POWER	GROUND
SPI_CS _n	21	DIGITAL IO	SPI chip select pin. Active Low.
SPI_MISO SPI_IO1	22	DIGITAL IO	Single SPI Mode: Slave to Master output from Total-EBR1553SPI. Dual SPI Mode: Input or Output data, even bit to Total-EBR1553SPI. Internal pullup.
SPI_IO2	23	DIGITAL IO	SPI IO2 for future quad SPI.
SPI_IO3	24	DIGITAL IO	SPI IO3 for future quad SPI.





Dual and Single SPI automatic detection

Total-EBR1553SPI Has a unique automatic detection of the SPI width. Total-EBR1553SPI starts after hardware reset in single SPI mode. If the SPI_MISO signal is detected as low during the first 2 SPI_CLKs of the SPI command, the SPI mode switches to Dual SPI. Once set to Dual SPI, Total-EBR1553SPI will stay in Dual mode until power down.

If Total-EBR1553SPI does not detect these two '0' bits, it will stay in single (standard) SPI mode.

Total-EBR1553SPI assumes that SPI mode is set to either single or dual and does not change.

Future versions of Total-EBR1553SPI will support Quad SPI with the same automatic detection. SPI_IO2 and SPI_IO3 will be used for quad SPI. SPI_IO3 is the MSBit.



Challenges with EBR1553 interface solutions

EBR1553 interface solutions provided on the market suffer from several issues. Sital Technology provides EBR1553 components and testers that solve these issues:

1. There is no formal validation testing for EBR1553 as there is for MIL-STD-1553 standard.
2. Some vendors implement EBR1553 Link mode with manually controlled Multiplexer for the BC HUB.
3. Some EBR1553 components & testers can only operate at bus wire's length of a few meters.

Missing Validation Criteria

An LRU equipped with MIL-STD-1553 is required to pass RT Validation before first air-born. This assures seamless interoperability between LRUs from different vendors. EBR1553 lacks the RT Validation, or any other type of validation. This gap created at least two dialects of EBR1553. Those dialects are somewhat different, such that interoperability between two LRUs with different dialects might fail communication.

→ Sital Technology's EBR1553 IP cores and Testers support both dialects.

→ Sital Technology's EBR1553 IP cores and Testers pass through a rigid set of validation tests that are extracted from the MIL-STD-1553 RT/MT/BC Validation test set.

EBR1553 Link mode

In EBR1553 BC HUB Link mode, each line/link serves messages for different RT address, for example link #3 would carry messages to RT3, however in link mode RT address in the command is changed to 0. In Sital's EBR1553 that is exactly what happens, transparent to the programmer. The programmer adds a BC message to RT3, and Sital's EBR1553 IP routes it through line 3, but also changes the RT address of the command to 0. Most other EBR1553 solutions out there relay on legacy MIL-STD-1553B chipset and do not change the RT address automatically, so their BC has to load the frame with command to RT address 0, and specify somehow, awkward, to route this message through link 3. But what happens if the next message is for RT2, can it do all these routing back to back...??? Probably not.

→ Sital's EBR1553 does all these conversions automatically, and uses the very same Enhanced Mini Ace API functions as for MIL-STD-1553. Fully transparent.

Line/Link maximum length

EBR1553 runs on RS485 physical layer instead of the floating MIL-STD-1553 standard. EBR1553 is point to point between the BC HUB and each of the RTs. Both ends are terminated by 120 Ohm.

It so happens that in some cases and for some vendors, their EBR1553 transmitters fail to properly shape their 10Mbps signaling, and communication fails.

For short bus wires lengths, it still works, but as the length extends, such as in a bigger weapon system on bigger aircraft, communication fails. Typically, we have seen communication fail at wires length longer than 12 meters.

However, it must be considered that failures at 12 meters experiences very low SNR at 10, 8 and 6 meters.

In Sital Technology we conducted a thorough analysis into their failure, understood the reason for it, and composed a robust EBR1553 transmitter receiver that performs well, with excellent SNR up to 50 meters of RS485 line/link. Our EBR1553 solutions are deployed in multiple applications with both dialects, flying since 2015.

[https://www.sitaltech.com/
EBR1553 IP page](https://www.sitaltech.com/EBR1553_IP_page)