BRD1553XVR-PMOD

MIL-STD-1553 transceiver and Transformer

With

PMOD adaptor

Hardware Interface Manual

USER'S MANUAL

Rev 8.2022

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1 KEY FEATURES AND BENEFITS

- Complete dual redundant MIL-STD-1553B transceiver and transformer
- Suitable for any MIL-STD-1553 BC, RT or MT application
- Works in conjunction with Sital's MIL-STD-1553/1760 IP cores
- Easily connects with PMOD header for most FPGA evaluation boards
- Standard MIL-STD-1553 Triax connectors.
- Single 3.3V supply operation
- Less than 0.3W maximum power dissipation during 1553 transmission
- RoHS compliant

2 ABOUT THIS MANUAL

This document is intended for users looking to interface from an FPGA board through a PMOD connector to a board with a dual MIL-STD-1553 transceiver and transformer and to a MIL-STD-1553 bus though a pair of 78 ohm twisted/shielded cables and triax connectors.

Figure 1: BRD1553XVR-PMOD Board without Cables

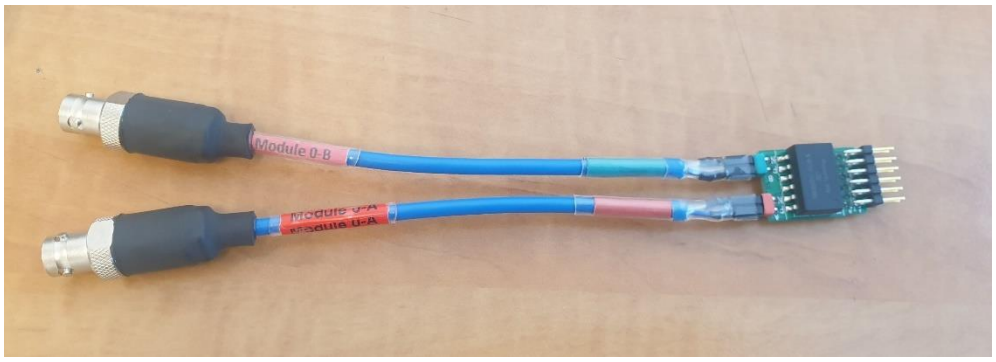

Figure 2: BRD1553XVR-PMOD Board with Triax Cables

3 BRD1553XVR-PMOD ADAPTOR BOARD SOLUTION

The BRD1553XVR-PMOD unit is intended for MIL-STD-1553/1760 applications, testing and evaluation of Sital's IP cores, transceivers and transformers and for users' software development.

Sital's BRD1553XVR-PMOD Adaptor Board is targeted to users developing MIL-STD-1553 applications requiring 1553 transceivers and transformers before their actual system's hardware is available. For such applications, the BRD1553XVR-PMOD can be used for the evaluation of Sital's 1553 IP and transceivers, or for software development.

The board contains the MIL-STD-1553 dual analog transceiver and dual isolation transformer. A buffering IP is required to interface between an FPGA or ASIC providing standard COTS transceiver signals and the BRM1553XCVR-PMOD. Sital's BRM1553D IP contains this IP and signaling. However, the user is required to add this buffering IP for situations involving the use of a different 1553 IP core or digital ASIC.

The BRM1553XCVR-PMOD can be easily connected to an FPGA development board using a standard PMOD header.

3.1 PMOD HEADER PINOUT

A standard PMOD header is a 12-pin header with 2.54mm pitch that's typically used for SPI interfaces and general purpose connections. PMOD connectors are commonly available on many FPGA development boards. It is a simple matter to build a working 1553 node with the digital IP inside the FPGA, and the BRM1553XCVR-PMOD board with the dual transceiver and transformer through the PMOD header.

BRD1553XVR-PMOD comes with a right-angle connector for its PMOD header interface. However, the BRD1553XVR-PMOD can be connected with a vertical header as well. These two connection methods would swap channel A and B. Swapping A and B is not an issue, since 1553 is indifferent, and since the user can swap the Triax cable connections of bus A and B in return, but nevertheless, a short description of the difference is described below:

3.1.1 VERTICAL CONNECTION

For Vertical PMOD connection please route channel A signals to pins on the left and channel B on the right.

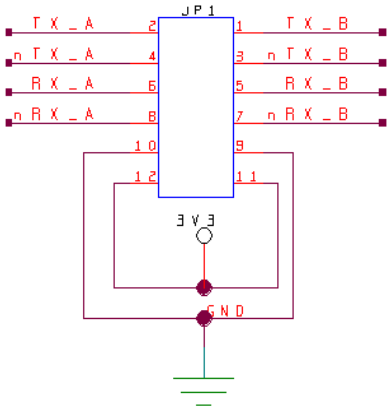

Figure 3: PMOD header pinout for vertical connections

3.1.2 RIGHT ANGLE CONNECTION

For right angle PMOD header connection please route channel B signals to pins on the left and channel A to pins on the right.

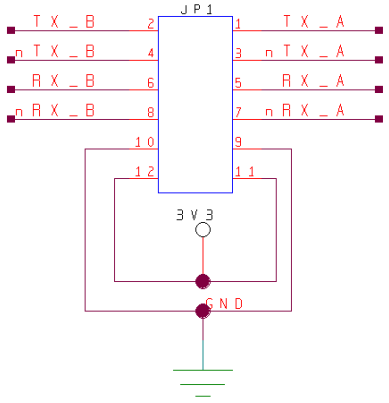

Figure 4: PMOD header pin-out for right angle connections

3.2 BUFFERING IP FOR BRD1553XVR-PMOD

The buffering IP is required for Mil-STD-1553 IPs that are NOT delivered by Sital Technology.

The buffering IP performs reshaping of the transmit signals to support the PMOD board's transmitter circuit.

The buffering IP also includes logic implementing a closed-loop means for re-timing the Channel A and Channel B transmitter signals in order to eliminate residual voltages (dynamic offset) caused by asymmetries between the transmitter's "+" and "-" output circuits, isolation transformers and loading by the 1553 bus and stub.

All transmissions by the PMOD board are echoed back from the MIL-STD-1553 bus to the board's 1553 receivers. However, for the case where there's a missing or significantly truncated echo, this indicates the presence of a short circuit on the stub or bus, or a transceiver malfunction. In this case, the transmitter will stop transmitting after approximately 500 ns.

The VHDL block diagram of Figure 4 shows the test bench for the buffering IP called XCVR_v8_xxx_Sital_OH.VHD

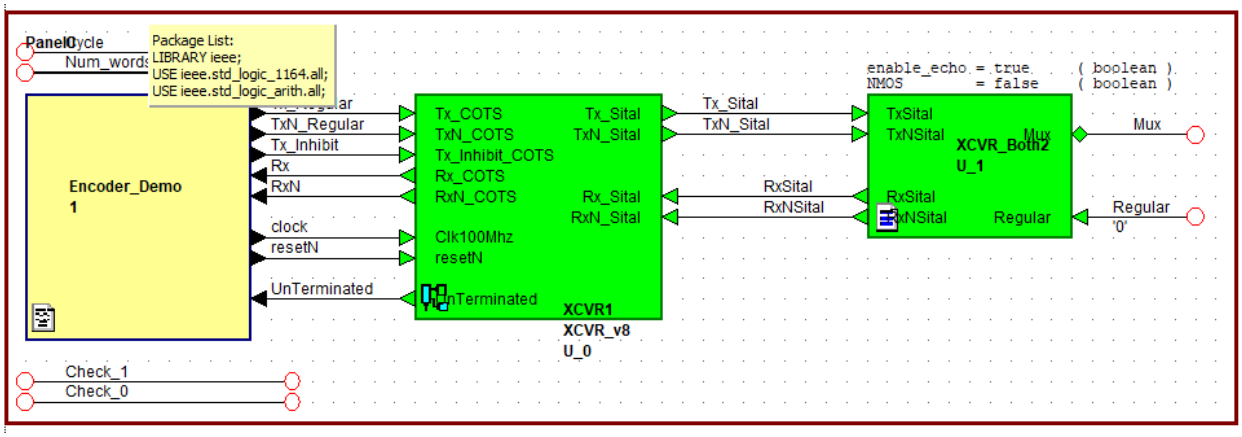

Figure 4: VHDL Block Diagram of non-Sital IP (yellow) Interfacing to Sital Transceiver on PMOD board.

In the user's design, this block, the green block in the center of Figure 4, needs to be instantiated in the FPGA between the standard COTS transceiver interface signals from the yellow block on the left side of Figure 4 to the left side of the buffer IP core (the center green block) and the FPGA signals on the right side of the center (green) block that route to the PMOD connector.

Please note that the 4 Sital Tx and Rx signals must be 3.3V I/O signals, and NO buffers may be used in this path.

Please contact Sital for any deviation.

3.2.1 BUFFERING IP FILES

The buffering IP is delivered in a ZIP file. Please unzip with the directory structure maintained.

The RTL_SRC directory contains 2 VHDL files. One is the netlist of gates, and the second is the VHDL description of the gates. These files are FPGA agnostic and be used with any available FPGA. Both are added to the synthesizer files.

The TB_SRC contains test bench files to simulate it in Modelsim VHDL simulator.

The root directory contains Modelsim script that would compile and simulate these files automatically.

4 DC AND SWITCHING CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS [1, 2]

Supply Voltage V_{CC}	-0.5 to 3.75V
Input or I/O Tristate Voltage Applied[3]	-0.5 to 3.75V
Storage Temperature (Ambient)	-65 to 150°C
Operating Temperature	-40°C to +85°C
Junction Temperature Under Bias (Tj)	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. All voltages are referenced to GND.
3. Overshoot and undershoot of -2V to (VIHMAX + 2) volts are permitted for a duration of <20 ns.

4.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Units
VCC	Board Supply Voltage	3.20	3.40	V
tJIND	Junction Temperature, Industrial Operation	-40	100	°C

4.3 DC ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions:

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Logic '1' Output Voltage		VCCIO - 0.4	-	-	V
VOL	Logic '0' Output Voltage		-	-	0.4	V
VIH	Logic '1' Input Voltage		2.0	-	3.6	V
VIL	Logic '0' Input Voltage		-0.3	-	0.8	V

5b Atir Yeda St., Kfar-Saba, ISRAEL 4464325

Email: info@sitaltech.com

Website: http://www.sitaltech.com