SIT-2579

Dual Compact MIL-STD-1553 or MIL-STD-1553/1760
Transceiver/Transformer Combo

Preliminary Data Sheet

Part Numbers

SIT-2579(-1760)	-40° C to +85° C
SIT-2579(-1760)-ET	-55° C to +125° C

SIT-2579 Dual MIL-STD-1553 Transceiver/Transformer Combo

Sital's SIT-2579 is a dual-channel MIL-STD-1553 or MIL-STD-1553/1760 transceiver/transformer combo. This integrated solution is based on the design of the SIT-1579 dual transceiver with the addition of a dual isolation transformer to provide transformer (stub) coupling. The transmitter for the SIT-2579-1760 version outputs a minimum stub voltage of 20 volts peak-to-peak, making it suitable for MIL-STD-1760 applications.

The SIT-2579 interfaces with 3.3V logic signals from an FPGA or digital ASIC instantiating one of Sital's MIL-STD-1553 IP cores. Based on discrete components, the SIT-2579 uses state of art power switching devices to reduce power dissipation to under 300 mW at 100% transmit duty cycle. This provides the lowest transmitter dissipation in the industry. In addition, no special thermal pads are required for mounting the device.

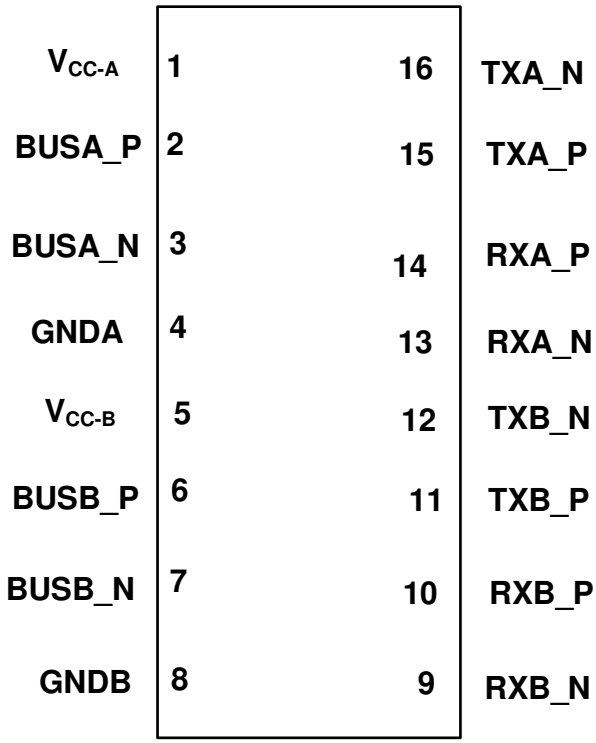
The SIT-2579 comes in a 16-pad leadless, surface-mount package.

The SIT-2579 transceiver operates in conjunction with Sital's 1553 digital IP instantiated in an FPGA or ASIC. By means of a real-time closed-loop correction technique, this enables the SIT-2579 to eliminate or minimize transmitter residual voltages, aka dynamic offsets or "tails" at the end of message transmissions. By allowing continuous adjustment to compensate for changes in power supply voltage and temperature, this technique provides improved performance over factory-trimmed transmitters. As a result, the SIT-2579 is ideal for applications requiring the transmission of a series of consecutive 32-word messages.

Key features of the SIT-2579 include:

- Compliance with MIL-STD-1553A and B
- SIT-2579-1760 version complies with MIL-STD-1760
- Operates from a 3.3V supply
- Lowest transmit power dissipation in the industry
- When transmitting, operates with Sital FPGA logic to provide a real-time, closed-loop mechanism to eliminate or minimize residual voltage "tails"
- 16-pad leadless flatpack
- Works with the following Sital IP Cores:
    - BRM1553D
    - DO254-BRM1553D
    - BRM1553FE
    - BRM1553PCI
    - BRM1553SPI
    - BRM1553ERL
    - BRM1553D-SnS

Package Pinout



Pinout: 16-pin Leadless Flatpack (top view)

Absolute Maximum Ratings

Parameter	Value
Supply Voltage (V_{CC-x})	-0.3V to +3.6V
Logic Input	-0.3V to +V_{CCX}
Receiver Voltage	30 V_{PK-PK}
Driver Current	700 mA
Reflow Solder	245 °C
Junction temperature	175 °C
Storage temperature	-65°C to +150 °C

Electrical Characteristics

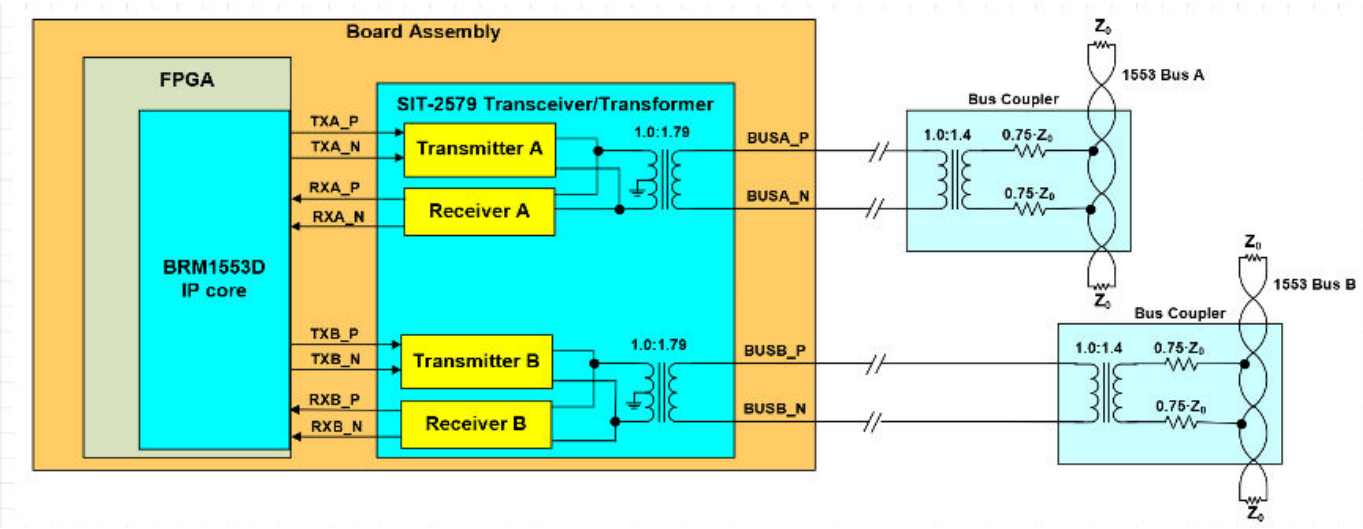
Parameter	Symbol	Condition	Min	Typical	Max	Units
POWER INPUT, POWER DISSIPATION						
Power Supply Voltage	V_{CC-A}, V_{CC-B}		3.15	3.30	3.50	Volts
Total Power Supply Current (total V_{CC-A} + V_{CC-B})	I_{CC1}	Non-transmitting		10	15	mA
	I_{CC2}	50% Transmit Duty Cycle		250	270	mA
	I_{CC3}	100% Transmit Duty Cycle		500	550	mA
Power dissipation (SIT-2579)	P1	Non-transmitting		30	60	mW
	P2	50% Transmit Duty Cycle		140	170	mW
	P3	100% Transmit Duty Cycle		250	280	mW
Power dissipation (SIT-2579-1760)	P1	Non-transmitting		30	60	mW
	P2	50% Transmit Duty Cycle		168	204	mW
	P3	100% Transmit Duty Cycle		300	336	mW
RECEIVER						
Differential input impedance	Z_{IN}	Transformer-coupled, 2V RMS signal, 75 kHz to 1 MHz, powered or unpowered	1.0			Khom
Receiver threshold voltage	V_{THRESH}	Maximum voltage for which receiver outputs remain inactive	0.200	0.550	0.860	V_{PK-PK}
Common mode voltage	V_{CM}	Common mode voltage, DC to 2 MHz, applied between BUSA(B)-P(N) and analog ground without disrupting receiver operation.	-10		10	V_{PEAK}
TRANSMITTER						
Differential Output Voltage (SIT-2579)	V_{DIFF}	V_{CC} = 3.30V, transformer coupled, Z_{LOAD} = 70Ω ohms, measured on stub	18	20	27	V_{PK-PK}
Differential Output Voltage (SIT-2579-1760)			20	22	27	V_{PK-PK}

Parameter	Symbol	Condition	Min	Typical	Max	Units
Output Offset Voltage	V_{OFFSET}	Transformer-coupled across 70 ohms	-250		250	mV_{PK-PK}, differential
Rise/fall time	$t_{RISE/FALL}$	Transition times between the 10% and 90% points of the peak-to-peak voltage	100	125	300	ns
LOGIC						
Logic high input voltage	V_{IH}		2.0			V
Logic high input current	I_{IH}		20		100	µA
Logic low input voltage	V_{IL}				0.8	V
Logic low input current	I_{IL}		-10		+10	µA
Logic high output voltage	V_{OH}	V_{CC-X} = 3.15V, I_{OH} = max	2.4			V
Logic high output current	I_{OH}				-3.4	mA
Logic low output voltage	V_{OL}	V_{CC-X} = 3.15V, I_{OL} = min			0.4	V
Logic low output current	I_{OL}		3.4			mA
THERMAL						
Thermal Resistance, Junction-to-Case	θ_{JC}					°C/W
Operating (case) Temperature	T_I	Industrial (SIT-2579)	-40		85	°C
	T_M	MIL-Part (SIT-2579-ET)	-55		125	°C
PHYSICAL CHARACTERISTICS						
Package Body Size (16-pad leadless package)			0.67 x 0.52 x 0.20 (17.0 x 13.2 x 5.1)			in. (mm)
Weight				0.282 (8)		oz (g)

Signal Descriptions

Pin Number	Symbol	Description
1	V_{CCA}	3.3 Volts input power supply for Channel A only.
2	BUSA_P	CH. A transformer positive side stub connection
3	BUSA_N	CH. A transformer negative side stub connection
4	GNDA	Ground for channel A only.
5	V_{CCB}	3.3 Volts input power supply for Channel B only.
6	BUSB_P	CH. B transformer positive side stub connection
7	BUSB_N	CH. B transformer negative side stub connection
8	GNDB	Ground for channel B only.
9	RxB_N	Output of CH. B inverted receiver logic output (to FPGA)
10	RxB_P	Output of CH. B non-inverted receiver logic output (to FPGA)
11	TxB_P	CH. B non-inverted transmit input logic signal (from FPGA)
12	TxB_N	CH. B inverted transmit input logic signal (from FPGA)
13	RxA_N	Output of CH. A inverted receiver logic output (to FPGA)
14	RxA_P	Output of CH. A non-inverted receiver logic output (to FPGA)
15	TxA_P	CH. A non-inverted transmit input logic signal (from FPGA)
16	TxA_N	CH. A inverted transmit input logic signal (from FPGA)

Connection Diagram



Functional Description

Transmitter Path

Sital's BRM1553D (or other) MIL-STD-1553 FPGA IP core provides two transmit signals, TXA(B)_P and TXA(B)_N, for each of Buses A and B. Unlike other COTS transceivers, the Tx Inhibit signal is not required for the transceiver/transformer since the transmit inhibit function is implemented

by the IP. If the transmission is inhibited by an external signal applied to the IP, the IP will deactivate the TXA(B)_P and TXA(B)_N signals.

Since Sital's MIL-STD-1553 IP uses 3-state (including high-Z) signaling for its digital transmitter signals, the transceiver/transformer's TXA(B)_P and TXA(B)_N input signals should be connected directly to the FPGA pins with no intervening buffers. If logic voltage level translation is required, please contact Sital Technology.

FPGA logic shapes the TXA(B)_P and TXA(B)_N signals such that the SIT-2579 transmits a properly shaped trapezoid signal with rising and falling edges of approximately 125 ns.

For the case where there's a short circuit in the SIT-1579's isolation transformer, the 1553 stub or coupling transformer, the SIT-2579 has built-in protection against overcurrent which limits the source current to 700 mA to prevent overheating. Once the short circuit condition is cleared, the transmitter continues with normal operation.

Receiver Path

The SIT-2579's receiver circuit contains an analog filter to reduce noise along with a comparator. The comparator circuit is designed to provide a receiver threshold of about 550 mV_{PK-PK}. For a transformer-coupled terminal, this is approximately midway between MIL-STD-1553B's minimum receiver threshold of 200 mV_{PK-PK} and maximum threshold of 860 mV_{PK-PK}.

Symmetry Alignment

During transmission, Sital's FPGA IP monitors the SIT-2579's RXA(B)_P and RXA(B)_N receiver outputs. In this way, the IP able to implement a continuous, closed-loop mechanism for maintaining symmetrical transmission. This involves modifying the transition timing for the FPGA's TXA(B)_P and TXA(B)_N outputs (transmitter inputs) to eliminate or minimize any residual voltage (aka dynamic offset or "tails") at the end of message transmission.

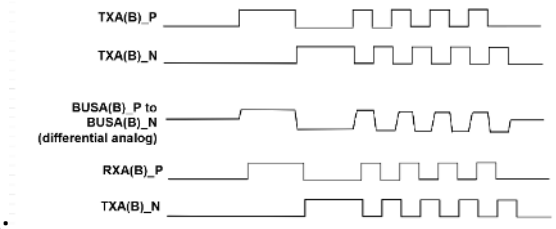
Other COTS MIL-STD-1553 transceivers are trimmed for symmetry during manufacture, a costly process resulting in expensive transceiver offerings with known performance symmetry issues. Moreover, these transceivers aren't able to make real-time adjustments to compensate for variations in temperature, power supply voltage, transformer variations or the effects of component aging and even intermittent wiring faults during flight.

This process is necessary because the push-pull switching circuit driving the two transformer primaries are never identical and tend to charge the bus based on differences between the two switches or the inductance values of the isolation transformer's primary half-windings. In most other COTS transceivers, this compensation process is mandatory and contributes significantly to component cost. The SIT-2579 and Sital MIL-STD-1553 IP implement a real-time correction loop in which the receiver and FPGA logic determine any asymmetry, thereby enabling transmitter logic to re-time the FPGA's TXA(B)_P and TXA(B)_N FPGA outputs to make the necessary adjustments. Sital's real-time symmetry alignment is a novel approach allowing for greater signal symmetry; improved performance over temperature, voltage and time; and easier design and development and at lower cost.

Safe and Secure

The SIT-2579 transceiver/transformer provides a companion solution to Sital's MIL-STD-1553 Safe and Secure (SnS) technology. By means of enhanced physical layer modeling, Sital's SnS can detect cyber authentication violations; that is, instances of "spoofing" (impersonating) BCs and RTs. In addition, SnS sensors can also detect and locate electrical faults such as intermittent or continuous open or short circuits in cables, connectors or LRUs. Sital also offers an adjacent technology called Force Multiplier (FMX). FMX provides a cloud-based application for collecting and reporting SnS data from all data buses on multiple aircraft and making the data available to ground maintenance personnel.

Transceiver/Transformer Timing



NOTES:

1. TXA(B)_P(N) are logic signals output from the FPGA to the SIT-2579 transmitters.
2. RXA(B)_P(N) are logic signals output from the SIT-2579 receivers to the FPGA.
3. The BUSA(B)_P to BUSA(B)_N voltages are differential analog signals measured across the 1553 data bus stub.

Outline Drawing

16-pad leadless flatpack