BRD1553SPI

HARDWARE MANUAL

Mil-Std-1553 terminal Board

USER'S MANUAL

Rev 3.5

October 2017 – Changed SPI read and write diagrams

November 2017 – Pin swap between bus A and B, Additional SPI mode

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1 DC AND SWITCHING CHARACTERISTICS

1.1 ABSOLUTE MAXIMUM RATINGS [1, 2]

Supply Voltage VCC	-0.5 to 3.75V
Input or I/O Tristate Voltage Applied[3]	-0.5 to 3.75V
Storage Temperature (Ambient)	-65 to 150°C
Operating Temperature	-40°C to +85°C
Junction Temperature Under Bias (Tj)	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. All voltages referenced to GND.
3. Overshoot and undershoot of -2V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.

1.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Units
VCC	Board Supply Voltage	3.20	3.40	V
tJIND	Junction Temperature, Industrial Operation	-40	100	°C

1.3 DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions:

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Logic '1' Output Voltage		VCCIO - 0.4	-	-	V
VOL	Logic '0' Output Voltage		-	-	0.4	V
VIH	Logic '1' Input Voltage		2.0	-	3.6	V
VIL	Logic '0' Input Voltage		-0.3	-	0.8	V

RoHS

2 INTRODUCTION

2.1 ABOUT THIS MANUAL

This document is the user's manual for BRD1553SPI daughter board, used to establish MIL-STD-1553B communication, and is controlled by an SPI channel. The card incorporate the BRM1553D IP as well as SPI interface block, dual discrete transceiver and two transformers. The pinout includes both coupling options, transformer or direct.

This manual describes the hardware interface to the boards.

Please refer to the BRM1553D IP HSID for detailed description of the modes of operation of the 1553 protocol IP.

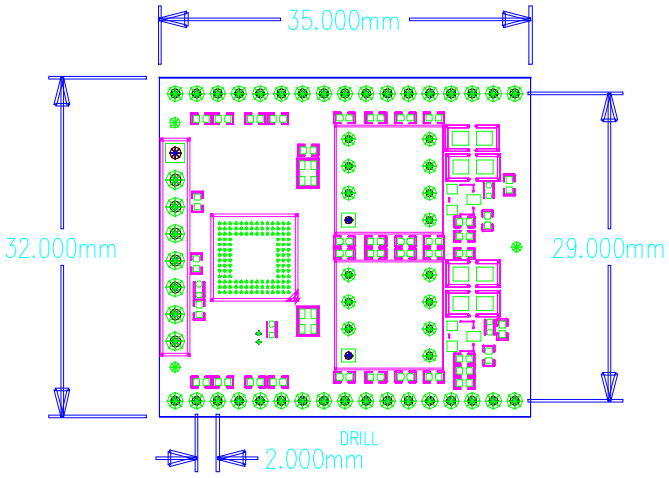

Figure 1: BRD1553XVR Board – Top View

2.2 THE BRD1553SPI BOARD

BRD1553SPI is a Mil-Std-1553 RT/MT or BC with SPI (Serial Peripheral Interface) backend interface.

This configuration enables a self-contained module with the 1553 protocol engine, transceiver and transformer for dual-redundant Mil-Std-1553 applications.

The unit communicates to a host CPU via SPI and is software compatible with other Sital products and with DDC Enhanced MiniACE devices.

The board is designed for extended temperature range of -40 to +85^{0}C and high mechanical sustainability. It is intended for use by customers who require a simple and cost-effective 1553 module on their system.

2.3 KEY FEATURES AND BENEFITS

- Complete Dual-Redundant Mil-Std-1553B Bus transceiver and transformer
- Suitable for any MIL-STD-1553 BC, RT, MT and specific applications
- Works in conjunction with Sital's Mil-Std-1553 IP cores
- Easily connects to most FPGA evaluation boards
- Single 3.3Vdc supply operation
- SPI interface, RT address, and interrupt pins for simple connectivity.
- Less than 0.3W maximum power dissipation during 1553 transmission (1.5W on load)
- 32 x 35mm (1.26 x 1.38 inch)
- Simple 2 pins connection directly to 1553 bus
- Simple Header connector to host board
- RoHS Compliant

3 BRD1553SPI FUNCTIONALITY

BRD1553SPI board is a fully functional, dual-redundant Mil-Std-1553 BC/RT and Monitor, with transceiver and transformer pair. It implements the Sital BRM1553D IP Core, transceiver design and transformer, which enables a quick and low cost integration into customer's designs. The BRM1553D IP is accessible through 4 wire SPI channel. The SPI interface supports up to 50 Mhz. Simple read and write operations are supported for memory and registers.

In addition, power, 1553 bus and Interrupt lines complete the pinout of the module.

The following drawing shows the board's schematics:

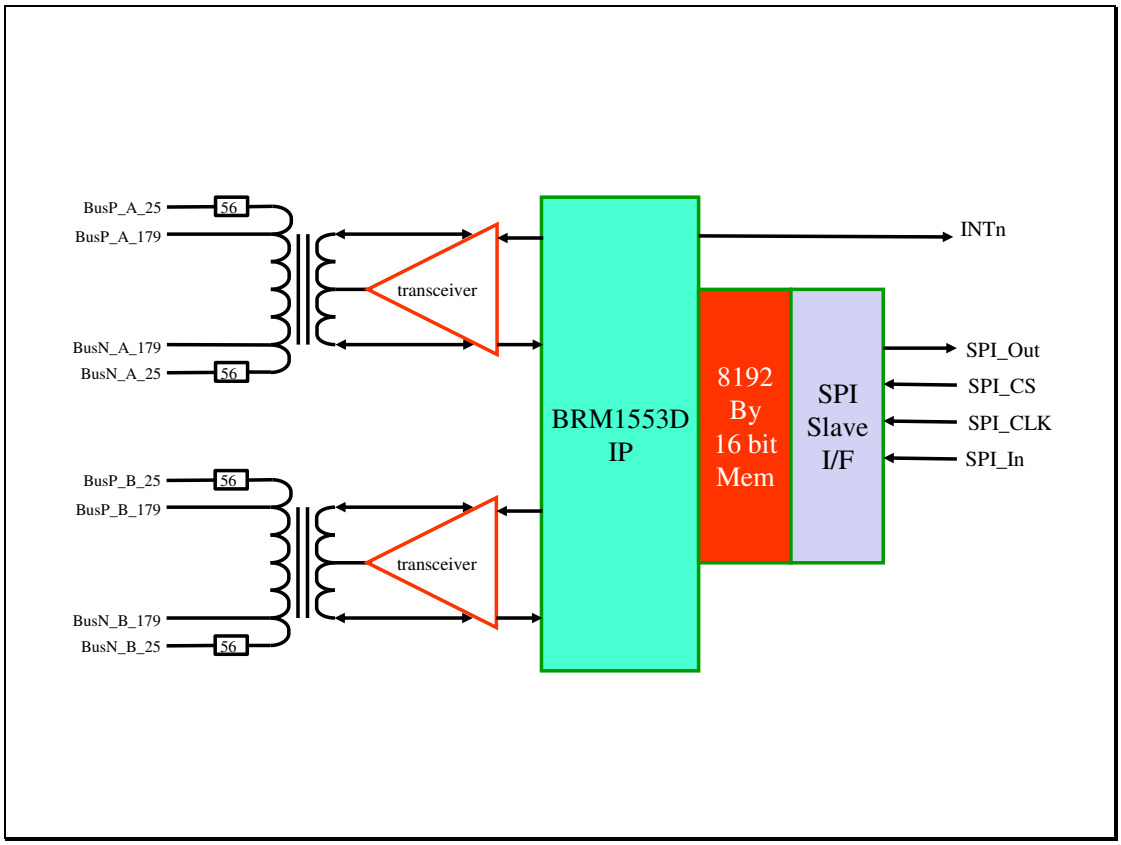

Figure 2: 1553 Protocol Engine Configuration

3.1 BRD1553SPI PINOUT

In this mode the card is connected with the Host through an SPI link. The SPI link supports SPI mode 0 and SPI mode 3. In these modes, the BRD1553SPI samples the SPI_In (MOSI) on the rising edge of the SPI_CLK, and sends the data on the falling edge (mode 0).

PCB Pin	Pin	Function	PCB Pin	Pin	Function
1	P1 - 1	3V3	34	P2 - 1	3V3
2	P1 - 2	N/C	33	P2 - 2	N/C
3	P1 - 3	N/C	32	P2 - 3	N/C
4	P1 - 4	GND	31	P2 - 4	GND
5	P1 - 5	N/C	30	P2 - 5	INTn
6	P1 - 6	N/C	29	P2 - 6	SPI_Out (MISO)
7	P1- 7	GND	28	P2 - 7	GND
8	P1 - 8	N/C	27	P2 - 8	SPI_In (MOSI)
9	P1 - 9	N/C	26	P2 - 9	SPI_CSn
10	P1 - 10	N/C	25	P2 - 10	SPI_CLK
11	P1 - 11	GND	24	P2 - 11	GND
12	P1 - 12	N/C	23	P2 - 12	N/C
13	P1 - 13	BUSN_B_179	22	P2 - 13	BUSN_A_179
14	P1 - 14	N/C	21	P2 - 14	N/C
15	P1 - 15	BUSP_B_179	20	P2 - 15	BUSP_A_179
16	P1 - 16	BUSN_B_25	19	P2 - 16	BUSN_A_25
17	P1 - 17	BUSP_B_25	18	P2 - 17	BUSP_A_25

Table 1: BRD1553SPI pinouts

The BRM1553SPI supports both transformer and direct coupling outputs. The user may choose to connect with the direct coupling outputs xxx_25 or the transformer coupling outputs xxx_179. P and N demote the Positive or Negative node of 1553 wiring, and the A and B letters define which bus.

Please note that some cards are delivered without the direct coupling mode serial resistors, and need to be specifically ordered.

3.1.1 RT ADDRESS SETTING

The RT address setting on the BRD1553SPI is done with software.

The process involves writing the RT address to configuration register 5 (address 9), and setting bit 5 of configuration register 6 (address 0x18) to ‘1’ to select RT address source. Please refer to BRM1553D HSID for details.

3.1.2 LAYOUT

Pin layout for top View

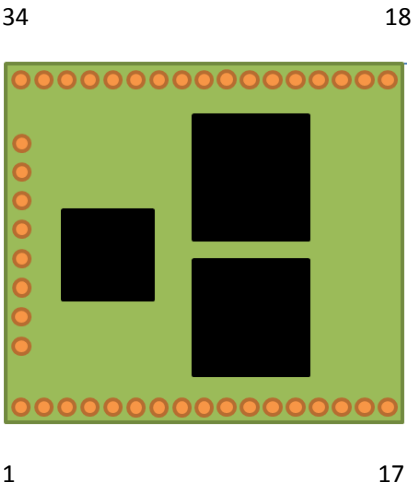

Figure 3:Board Layout

Please note that the side connector is meant for flashing and testing and should not be connected at customer board. This connector may be removed or cut if needed.

3.2 MEMORY MAPPING OF BRD1553SPI

Address 0 to 0xFFFF is Memory.

Address 0x10000 to 0x1001F is EMA register space

Address 0x10100 to 0x101FF is Sital Smart Wiring Technology (SWT) when implemented.

Examples:

Write 0x1234 to address 0xFF00: 0x0FF00**8**1234

Write incremental data to register 8 and up: 0x10008**8**0001000200030004…

Read 0x1234 from address 0xFF00: 0x0FF00**0**xxxx and read 0x1234 on the SPI_Out lines.

Read Incremental data from register 8 and up: 0x10008**0**xxxxxxxxxxxxxxxx, and read 0001000200030004

3.3 SPI SIGNALING

The SPI signaling supports serial read and write operations. The address space supports both the Registers and the memory.

SPI_CSn is normally high, and when it goes low, it initiates the transaction. When high it is treated as reset to the SPI block inside the BRD1553SPI.

To support fast clock data read, the command address phase is reversed compared with most other SPI signaling. The first 3 bytes sent MSB first from the master define the address and the command. The first 20 bits define a WORD address (as opposed to byte address), followed by 4 bits that define the command.

Read command: 20 bits of address, MSB first, followed by 4 bits of 0. So read from address 0 would be 0x000000.

Write command: 20 bits of address, MSB first, followed by 4 bits of 0x8. Write to address 0x100 would be 0x001008.

14 other possible commands are treated as read commands, until defined differently.

The data for the read or write commands follow the 4 bit command, either on the SPI_In (for write) or SPI_out (for read) depending on the type of command. The length of the data payload is defined by the master, and can be endless. Only multiples of 16 bit words are supported. Partial word length is not written.

3.3.1 BYTES SWAP (ENDIAN) CONTROL

Notice that the default bytes order of SPI data is MSB0 LSB0, MSB1 LSB1. This reflects the 16 bits words format of the BRM1553D IP. This order might confuse a typical SPI master which works in bytes order, assuming LSB0 MSB0, LSB1 MSB1…

Bit 19 (MSB of address) is used to swap each of the 2 bytes of each of the 16 bit words when high. When low, no swap is performed.

When no swap is performed, and assuming the SPI master works on bytes basis, and BRM1553SPI works on word basis, a swap of high and low byte would occur for all words, which would result in the inability to write proper data or read correct data.

When swap is performed by the BRM1553SPI, the first 8 bits of the data are the LSBs, while the second byte is the MSB.

For example of no swapping:

If the data in register 5 (time tag counter) in the BRD1553SPI is 0x1234 then the read command and returned data would appear on the SPI data lines as follows:

SPI_In (MOSI): 100050 -- --

SPI_Out(MISO): 0000000 12 34

An SPI master typically working in byte mode, would treat the first byte (0x12) as the LSBs, and the second byte (0x34) as the MSB, thus passing 0x3412 to the application layer, which is a mistake.

To overcome this issue, one can swap the bytes before writing and after reading, but the BRD1553SPI provides this feature by setting the address MSB to '1' for all transactions that require swapping, thus the above cycle would look like this:

SPI_In (MOSI): 900050 -- --

SPI_Out(MISO): 0000000 34 12

Using auto SWAP feature would relieve the SW from tedious data massaging which require lots of SW resources.

Verifying Proper Endian can be done by reading register address 0x13. Please verify that the value read is 0x7654.

3.3.2 SPI TIMING OPTION 2

It was noted that for several SPI controllers, the master read cycle did not support the BRM1553SPI response, and the data read was "multiplied by 2". BRM1553SPI thus supports an additional mode of operation for these cases that would read the right data.

If you read from register 0x13 the value 0xECA8, then you need to choose option 2.

Set address bit 18, (second bit sent) to '1' in order to read 0x7654.

Original SPI command: 100130 replies with 0xECA8

Updated SPI command: 500130 would reply with 0x7654.

3.4 SPI SIGNALS TIMING

3.4.1 BRD1553SPI WRITE OR READ CYCLE

The BRD1553SPI samples the SPI_IN bits at the rising edge of the SPI_CLK.

The BRD1553SPI outputs data on the SPI_Out on the 7 ns after falling edge of the SPI_CLK.

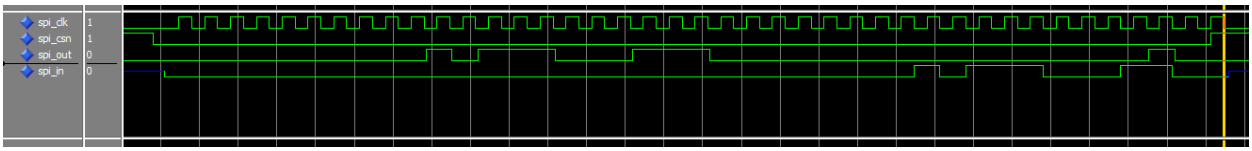

Figure 4: SPI write cycle example

The above figure displays a write cycle to memory address 0x2E3 data 0x0002, while SPI data in outputs irrelevant data, but shows timing during simulation (not showing the 7 ns output delay).

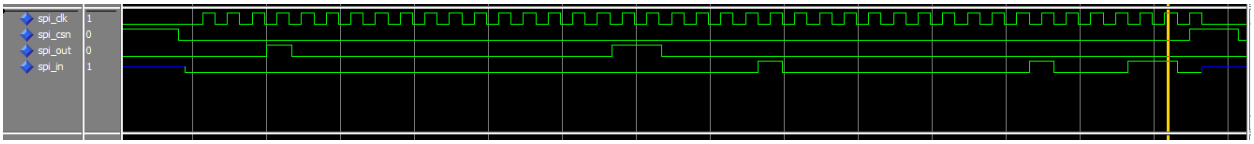

Figure 5: SPI Read cycle register address 0x6, data

The above figure displays a read cycle from interrupt status register address 6, with data return of 2.

Maximum SPI clock is 50 Mhz.

3.5 SPI PERFORMANCE

When selecting an SBC (Single Board Computer) to host the BRD1553SPI one must make sure that the SPI data access is fast enough to meet the 1553 performance required.

It has been observed with a number of SBCs that while the SPI clock is very fast, the latency between two such fast accesses is very long. For some reason the SPI UART can shift the address-data at very high speed, but it takes a long while to arrange a second access.

A good approach to test this access throughput is to read the time tag register 5 repeatedly inside the SBC. The time tag increments every 64 us (by default), so reading twice with difference of 2, implies that the two access operations were between 64 us and 128 us apart from each other. However, if 16 consecutive reads reveal the same value, it implies that the read rate is in the range of 4 us.

Assuming the 1553 bus activity that needs to be tracked (pass through SPI) is 30% of bus traffic, and bus traffic is 80% of the time @ 1 Mhz, one would need 1000000x0.8x0.3=> 240,000 bits per second => 15,000 Words per second => 66 us per access.

In case all traffic is captured, then 1Mx0.8/16 => 20 us per access is essential.

3.6 BOARD MECHANICS

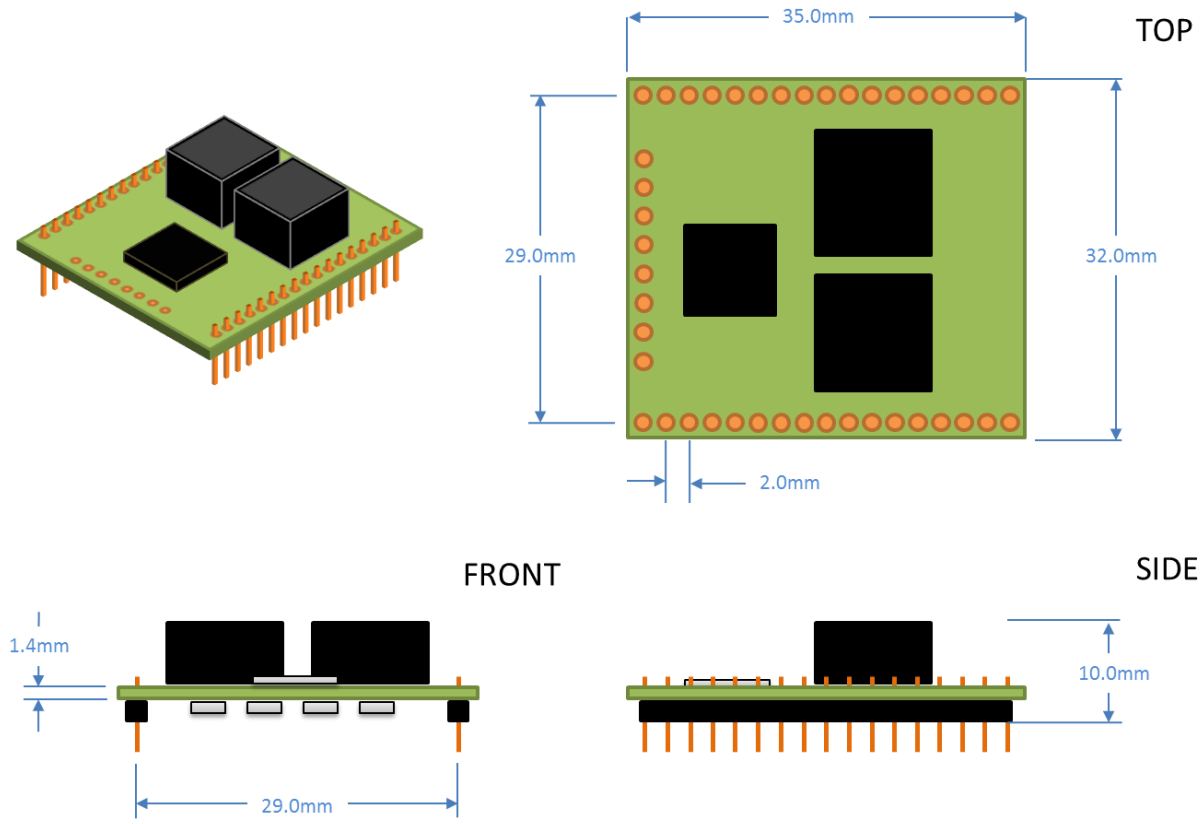

Figure 6: Board Mechanics

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