ARINC-429 Multiple Transmitters and Receivers IP Core

User's manual

Version 2.1

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Table of Contents

ARINC-429 IP Core

Overview

Version 2 of Sital's ARINC-429 IP core bundles up to 16 transmitting channels and 16 receiving channels with a single 32-bit host CPU interface.

This version of the ARINC-429 IP core is based on a unique approach for its compact RTL (Register Transfer Logic) description in which flip-flops from the previous version are replaced by memory elements. This coding approach is FPGA-architecture friendly by supporting 16 flip-flops in a LUT inside a memory cell, as opposed to using a single flip-flop for each FPGA cell. This enables a potential reduction by a factor of up to 16 in the amount of required logic resources.

In addition, the FIFOs for all transmit and receive channels share a common FPGA memory block. This allows for usage of a single memory element for 16 transmitters instead of 16 separate FIFOs. In the previous version, if each FIFO element used only a partial memory element, this would result in a large amount of unused memory resources.

Figure 1 shows the supplied Test bench example.

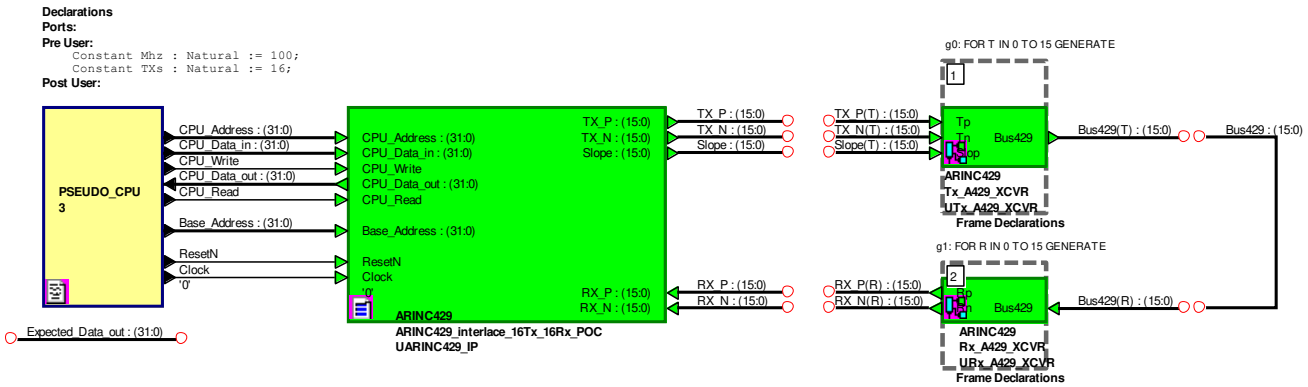

Figure 1. Test Bench Example

Configuration

The IP core should be configured for synthesis with the following parameters:

1. Clock Frequency – the clock input frequency used. A single clock input is used for the entire IP. This clock has to be in the same clock domain as the host accessing the IP, since the interface for input and output data is fully synchronous.
2. Number of transmit channels – must be defined 0 to 16.
3. Number of receive channels – must be defined 0 to 16.
4. Transmitter's FIFO depth – Depth of the FIFO for each transmitter channel. This depth must be a power of 2. The default value is 32.
5. Receiver's FIFO depth – Depth of the FIFO for each receiver channel. This depth must be a power of 2. The default value is 32.

Note that there is no option for hardware message filtering based on message label. This filtering was moved to the software reading the data words.

Run time configuration

When setup to run, each transmit IP must be configured for:

1. High (100 kb/s) or low (12.5 kb/s) baud rate.
2. With or without Parity insertion.
3. Odd or even parity.

When setup to run, each receive IP can be configured to:

1. High (100 kb/s) or low (12.5 kb/s) baud rate.
2. With Parity checking, or without. A message with wrong parity is rejected.
3. Odd or even parity.

Bit sequencing

The 32 bits that the user writes to the transmit FIFO are manipulated in accordance with the ARINC-429 standard. The bit ordering for the Message labels (8 LSBs), which are transmitted first, are swapped before transmission. For a 32 bits word with bits 31...0 written to the transmit FIFO, bit 7 is transmitted first, then 6 down to 0, and then bit 8, and 9 and up to bit 31. Parity bit, if enabled is set to bit 31.

The receiver is familiar with this trick, and it swaps the bits back to their original order upon arrival.

Error Message Filtering

Parity is the only hardware error handling available. Additional filtering can be done at the software level.

If parity is used, for the transmitting channels, the parity bit can be generated automatically by the IP hardware such that bit 31, the MSB, is replaced by the parity calculation of the 31 LSBs. In this case, the user MSB is dropped.

If Parity generation is not enabled in hardware, the user can compute the parity bit value in software.

If a receiving channel is configured to check parity, and the parity check fails, the failed word is filtered out and not stored in the receive FIFO.

IP Memory Mapping

The following is the memory mapping for the IP:

Byte Address	Mapped area contents
User Defined "Base_Address"	Base Address – 32 bits that define the base address of the ARINC-429 IP core. Bits 9:0 are assumed to be '0' and are ignored. All addresses below are offset from the Base address.

Address Offset	Each ARINC-429 Transmitter Channel
0x3:0x0	Transmit Data – 32-bit data to transmit. LSB is bit 0, MSB is bit 31.
0x4	Transmit Control: Set prior to transmission Bit 0 – Transmit Baud rate: '1' for 100Khz, '0' for 12.5Khz. Bit 1 – Insert Parity: '1' to enable transmit parity. Bit 2 – Polarity of parity – '1' for Odd Parity, '0' for even parity.
0x6	Read number of words in the transmit FIFO. Value = 0 to 255.
0x7	Bit 0 – When '1', this indicates that the Transmit FIFO is full. Bit 1 – When '1', this indicates that the Transmit FIFO is empty.
0x10-0x17	Same as above for 2nd transmitter
0x20-0x27	Same as above for 3rd transmitter
0xN0-0xN7	Same as above for Nth transmitter. N in range 0 0xF.

Address Offset	Each ARINC-429 Receiver Channel
0x103-0x100	Read received Data – 32-bit data from FIFO. LSB is bit 0, MSB is bit 31.
0x104	Transmit Control: Set prior to transmission Bit 0 – Transmit Baud rate: '1' for 100Khz, '0' for 12.5Khz. Bit 1 – Insert Parity: '1' for parity insertion enabled. Bit 2 – Polarity of parity: '1' for Odd Parity, '0' for even parity.
0x106	Read number of words in the Receive FIFO. Value = 0 to 255.
0x107	Bit 0 – Transmit FIFO Full when '1'. Bit 1 – Transmit FIFO Empty when '1'.
0x110-0x117	Same as above for 2nd receiver
0x120-0x127	Same as above for 3rd receiver
0x1N0-0x1N7	Same as above for Nth receiver. N is in range 0-0xF.

IP Ports Description

Figure 2. Block Diagram

Signal Name	length	I/O	Description
TX_P	16	Out	Positive serial data out to Line Driver. Bit 'X' in vector is for channel 'X'.
TX_N	16	Out	Negative serial data out to Line Driver Device. Bit 'X' in vector is for channel 'X'.
Slope	16	Out	Control the slope of the ARINC-429 Line Driver differential output signal. '1' – Line driver rise and fall times are 1.5µs. '0' – Line driver rise and fall times are 10 µs. Bit 'X' in vector is for channel 'X'.
RX_P	16	In	Positive serial data input from analog receiver. Bit 'X' in vector is for channel 'X'.
RX_N	16	In	Negative serial data input from analogue receiver. Bit 'X' in vector is for channel 'X'.
Clock	1	In	Clock in. Must be in clock domain of host.
ResetN	1	In	An active low signal that asynchronously resets all of the FFs in the core. Once ResetN is de=asserted, operation starts.
Base_Address	31:0	In	Base Address – 32 bits that define the base address of the ARINC-429 IP core. Bits 9-0 are assumed to be 0 and ignored.
CPU_Address	31:0	In	Read or write address.
CPU_Write	1	In	Level type write enable input.
CPU_Data_in	31:0	In	Data written to IP core. Data is written on the rising edge of the clock input when CPU_Write is '1'.
CPU_Data out	31:0	Out	Data read from IP. Data is ready on the following clock cycle after the IP core samples the CPU_Address.

Signal Name	length	I/O	Description
CPU_Read	1	In	Level type input to read data from the IP core. Since reading data is from a FIFO, burst is not supported. Data_out is available one clock cycle after CPU_Address and CPU_Read are sampled by the clock input.

ARINC-429 Overview

General Description

The ARINC-429 specification defines the standard requirements for the transfer of digital data between avionics systems. The standard is most commonly used on commercial aircraft.

ARINC-429 bus hardware consists of a single transmitter connected to between 1 to 20 receivers. Data is transmitted in one direction only. Transmission from the transmitter is comprised of 32-bit words containing a 24-bit data portion (containing the actual information), and an 8-bit label (identifying the data).

ARINC-429 employs unidirectional transmission of 32-bit words over two-wire twisted pairs using bipolar RZ format. Messages are transmitted at a bit rate of either 12.5 or 100 kb/s to other system elements which are monitoring the bus messages. Sequential words are separated by at least four bit times of null or zero voltage. By utilizing this null gap between words, a separate clock signal is unnecessary.

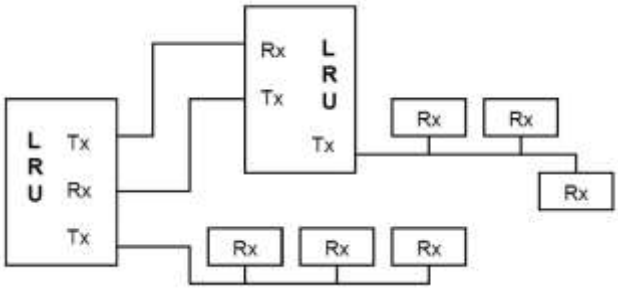

Figure 3. ARINC-429 Buses

ARINC-429 Characteristics

The transmission bus media uses a 78-ohm shielded/twisted pair cable. The shield must be grounded at each end and at all junctions along the bus.

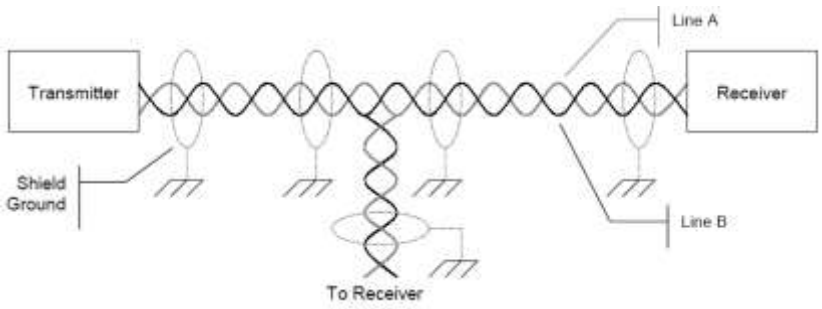

Figure 4. ARINC-429 Bus Connections

The transmitter's source output impedance must be 75Ω ± 5Ω divided equally between Line A and Line B. This balanced output should closely match the impedance of the cable. Receiving nodes sink must have a minimum effective input impedance of 8 kΩ minimum.

Maximum cable length is not specified, as it is dependent on the number of receivers, the receivers' drain and transmitter source power. Most systems are designed for under 150 feet, but conditions permitting, ARINC-429 cable lengths can extend to 300 feet and beyond.

ARINC-429 specifies two speeds for data transmission. Low speed operation is defined as 12.5kHz, with an actual allowable range of 12 to 14.5 kHz. High speed operation is 100 kHz ± 1%. These two data rates cannot be used on the same transmission bus.

Data is transmitted in a bipolar, Return-to-Zero format. This consists of a tri-state modulation consisting of HIGH, NULL and LOW states. Transmission voltages are measured across the output terminals of the source.

Transmit & Receive voltage:

TRANSMIT	STATE	RECEIVE
+10.0 V ± 1.0 V	HIGH	+6.5 to 13 V
0 V ± 0.5V	NULL	+2.5 to -2.5 V
-10.0 V ± 1.0 V	LOW	- 6.5 to -13 V

Bit Encoding Example:

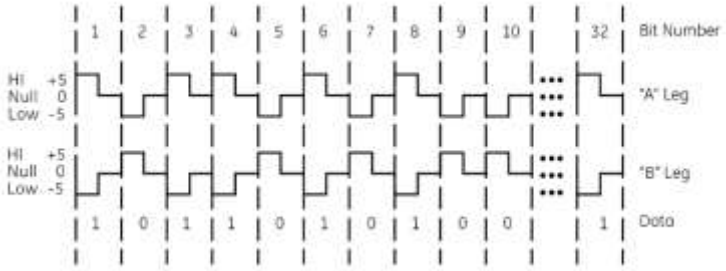

Figure 5. ARINC-429 Signaling

Parameter	High Speed	Low Speed
Bit Rate	100K bits/second	12.5K-14.5K bits/second
Time Y (one bit)	10 µsec ± 2.5%	1÷(bit rate) µsec ± 2.5%
Time X	5 µsec ± 5%	Y/2 µsec ± 5%
Pulse Rise Time	1.5 ± 0.5 µsec	10 ± 5 µsec
Pulse Fall Time	1.5 ± 0.5 µsec	10 ± 5 µsec

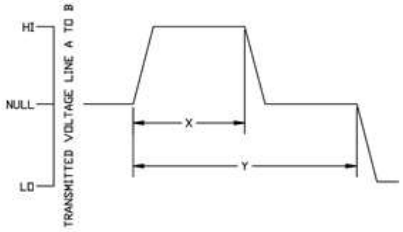

Figure 6. ARINC-429 Slew Rates and Bit Timing

ARINC-429 Word Format

ARINC-429 is a very simple, one-way point-to-point or point-to-points (broadcast) protocol. There can be only one active transmitter on a wire pair. The transmitter is always transmitting either 32-bit data words or is in the NULL state. There is at least one receiver on a wire pair; there may be up to 20.

In most cases, an ARINC-429 message consists of a single data word. The label field of the word defines the type of data that is contained in the remainder of the word.
ARINC-429 data words are 32-bit words made up of five primary fields:
> Parity – 1 bit
> Sign/Status Matrix (SSM) – 2 bits
> Data – 19 bits
> Source/Destination Identifier (SDI) – 2 bits
> Label – 8 bits

The ARINC-429 convention is to number the bits from 1 (LSB) to 32 (MSB):

Figure 7. ARINC-429 Word Formatting

The only two fields definitively required are the **Label** and the **Parity bit**, leaving up to 23 bits available for data representation.

Parity - The MSB is always the parity bit for ARINC-429. Parity is normally set to odd.

SSM - Bits 31 and 30 contain the Sign/Status Matrix or SSM. These two bits are defined differently depending on the format used of the data.

Data - Bits 29 through 11 contain the data, which may be in a number of different formats.
In some cases, the data field can overlap with the SDI bits. In this case, the SDI field is not used.

SDI - Bits 10 and 9 provide a Source/Destination Identifier.

Label - Bits 8 through 1 contain a label identifying the data type and the parameters associated with it. The label is used to identifies the type of data type transmitted in the remainder of the

word and, therefore, the method of data formatting uses. Labels are typically represented as octal numbers.

When transmitting data words on the ARINC-429 bus, the Label is transmitted first, MSB first, followed by the rest of the bit field, LSB first. Bit transmission order is as shown in Figure 8.

8, 7, 6, 5, 4, 3, 2, 1, 9, 10, 11, 12, 13 … 32.

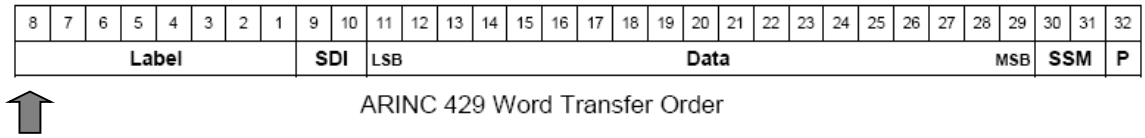

Figure 8. ARINC-429 Bit Ordering