SPI-to-MIL-STD-1553 IP Core





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BRM1553-SPI SPI-to-MIL-STD-1553/1760 IP Core

1553 Bus Controller, Remote Terminal and Monitor Terminal Implementation with SPI Target Interface

Compact, Robust, Reliable MIL-STD-IP-Cores

Key Features and Benefits

- MIL-STD-1553 Intellectual Property for FPGAs and ASICs
- Provides 1553 BC, RT, MT and RT/MT operating modes
- Architecturally compatible with *DDC[®] Enhanced Mini-Ace[®]* and *Micro-Ace[®]* and works with Sital API/library/driver software
- 4-wire SPI serial target interface.
- Operates at SPI data rates up to 50 Mb/s
- User can optimize RAM size between 4K x 16 and 64K x 16
- Small FPGA resource utilization
- Supplied with dual MIL-STD-1553 transceivers and isolation transformers
- Modular architecture allowing flexible implementations to minimize FPGA footprint
- Provided as vendor and technology independent VHDL netlist code
- SPI Master IP core available for host interface



Sital Technology's BRM1553-SPI IP core, transceiver and transformer provide an ideal solution for interfacing between a processor with a SPI port and a dual redundant MIL-STD-1553 bus. Designed from the ground up for use in aerospace, avionics and military MIL-STD-1553 solutions, the BRM1553-SPI, like all of Sital's MIL-STD-1553 IP cores, offers a uniquely compact, robust and reliable BC, RT, MT solution for any PLD/FPGA or ASIC device. All of Sital's 1553 IP cores were developed based on the company's unflagging commitment to quality and excellence with strict adherence to meeting the stringent requirements of military and aerospace specifications.

The BRM1553-SPI IP core is based on Sital's popular flagship BRM1553D MIL-STD-1553 core and provides the same register and memory hardware/software interface. For support of the BRM1553-SPI core, Sital offers API/library/driver software. Sital's MIL-STD-1553 software consists of over 150 low-level and high-level function calls for use in BC, RT, Monitor or RT/Monitor modes. Sital can provide its API/library with OS drivers for VxWorks 6.9, 7.0 or 653; Linux 3.0, LynxOS, Pico/Linux or Petalinux; Windows; PikeOS, Green hills Integrity or bare metal (no OS). The software is provided with API/library documentation and sample programs.

For programs requiring DO-254 and DO-178 certifiability, Sital is able to provide its BRM1553-SPI IP core and software drivers with certifiability at design assurance levels up to and including DAL A. Another option Sital offers is its Safe and Secure (SnS) technology. By means of enhanced physical layer monitoring, Sital's SnS is able to detect cyber authentication violations (i.e., impersonation or "spoofing") and detect and locate intermittent or continuous open and short circuit wire faults.

Specifications Compatibility

- Protocol IP, and dual transceiver and transformer provide full compliance with MIL-STD-1553B Notice 2 and MIL-STD-1760
- DDC® Enhanced Mini-ACE®/Micro-ACE/Total-ACE® Register bits/Memory Architecture
- Includes synthesis options for BC-only, RT-only, Monitor-only, BC/Monitor, BC/RT, RT/Monitor and BC/RT/Monitor

Host Interface

 SPI target interface operates at data rates up to 50 MHz and supports streaming

RAM (BRM1553PCI & BRM1553D)

- 4, 8, 16, 32, 64K x 16-bit Dual Port RAM (Limited by FPGA resources only)
- Includes RAM parity generation and checking

Clock

 Operates with an IP clock input frequency of 128 MHz

Supported FPGAs

- Any FPGA with sufficient number of LUTs and Dual-Port memory
- FPGA families from the following suppliers: Xilinx, Intel/Altera, Lattice, and Microsemi

* For other FPGAs or ASICs, please consult Sital

Deliverables

- VHDL netlist for the desired clock frequency
- Hardware and Hardware/Software Interface Document (HSID) user manuals
- Sample VHDL code that incorporates the core
- Test bench VHDL code
- Synthesis script for sample code
- Transceivers and transformers

Part Numbers:

- Development license: BRM1553-SPI-RND
- Per-instantiation license hardware key: BRM1553-SPI-HWLIC

Drivers for BRM1553-5MHz

- Windows XP 32Bits
- Windows 7, 8, 8.1, 10 32 & 64Bits
- Linux 32 & 64Bits:
- P/N: DRV1553LNX-32-64
 VxWorks 7.0:
- P/N: DRV1553VXW-7.0 • Others
- Others

SPI-to-MIL-STD-1553 IP Core

Clock Input and Manchester Decoder

Sital's unique Manchester decoder can work with a clock of any frequency and reduces the number of on-board clock domains, thereby reducing EMI/RFI. The decoder's advanced algorithms for filtering out noise and disturbances enable the core to operate reliably in the harshest environments.

BC Architecture

- Highly Autonomous BC, with Built-In Message Sequence Control
- Frame Scheduling
- Branching
- Asynchronous Message Insertion
- General Purpose Queue
- User-defined Interrupts

RT Architecture

- Options for Subaddress Single, Double and Circular Buffering and Global Circular Buffering
- Interrupt Status Queue
- 50% Circular Buffer Rollover Interrupts

Monitor Architecture

- Selective Message Monitor
- Filtering based on Address, T/R Bit, and Subaddress
- Separate Command and Data Stacks
- 50% and 100% Stack Rollover Interrupts

Transceiver and Transformer

- Trapezoidal transmitter waveform in accordance with MIL-STD-1553
- Low-power transceiver, with less than 300 mW transmitter power dissipation at 100% transmit duty cycle
- Real-time, closed-loop mechanism to continuously eliminate residual voltage; aka "dynamic offset" or "tails"
 - Transceiver and Isolation Transformer meet all MIL-STD-1553 requirements for waveform, isolation, noise rejection and common mode rejection

Sital Technology Ltd.



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Verification and Validation

To ensure a fully reliable and robust product the core was developed using an advanced verification environment that includes a random-generation engine, code-coverage and assertion tools.

All 1553 protocol, functions and performance requirements were verified.

Third Party Validation

Sital's MIL-STD-1553 IP cores have successfully passed the full MIL-STD-1553B Notice 2 RT Validation test, based on the test plan from MIL-HDBK-1553A.

Validation tests were performed by an independent third-party laboratory.

Simple Integration

To simplify the integration of the core, a sample VHDL design that uses the core is provided, along with:

- Comprehensive user's manuals.
- A VHDL gate level model of the core.
- A simulation script for compiling and running the core.
- A test bench that instantiates all of these components to a working example. This includes a bus tester VHDL model that generates 1553 messages and checks the responses.
- The test bench also includes a bus transceiver VHDL model that connects the core with 2 simulated buses.

FPGA Integration

Sital also offers an option for performing customers' on-FPGA integration. Sital's SVIVADO integration service provides an IP firmware and software solution by integrating its 1553 IP core with an on-chip processor using Xilinx's Vivado design suite. For the BRM1553-SPI, this integration includes the IP core, the SPI interface, an on-FPGA processor, Sital's API library software and the software drivers for the operating system and SPI interface.

About Sital

Sital Technology provides world-class products and expertise for communication bus applications in the avionics, aerospace and automotive industries. Sital embeds its vast experience and proficiency in its products, which include MIL-STD-1553 IP cores, components, boards and testers, as well as CAN bus devices IP and software. With its highly-experienced staff of experts, the company's Projects Division undertakes design, integration and turn-key engagements on behalf of the world's leading commercial and military avionics companies, space agencies, and automobile designers and manufacturers. Sital's bus technologies and expertise improve robustness and efficiency as they lower cost, space and resource utilization.

Sital's formidable customer list includes leading military and commercial organizations throughout the world, including: NASA, Boeing, Lockheed-Martin, Honeywell, Raytheon, General Motors, British Aerospace, Thales, ECIL(India), Aselsan, Elbit, Rafael and IAI.