



## **SVIVADO Turnkey Development Solution for MIL-STD-1553/1760**

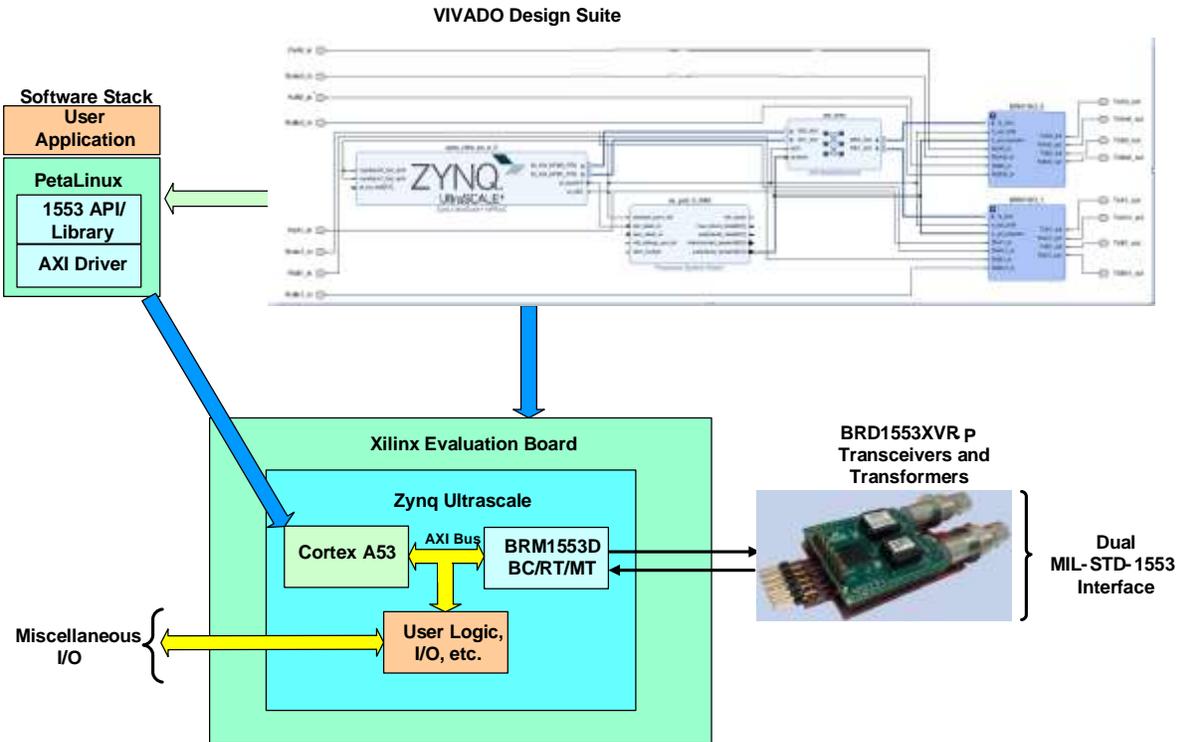
Sital Technology offers its SVIVADO integration package as a turnkey solution for integrating its MIL-STD-1553 or other IP cores and accompanying software on to a System-on-Chip (SoC) and Multi-Processor-System-on-Chip (MPSoC) FPGA. SVIVADO enables design efforts that in the past would take 6 to 12 months can now be accomplished in a matter of weeks or even days. This greatly accelerates times-to-market by facilitating the integration of disparate circuit elements, performing high-level logic synthesis using C, C++ and MATLAB, and enabling the parallel development of hardware and software.

For customers of Sital Technology's MIL-STD-1553 and other IP cores, Sital offers its SVIVADO service for integrating one of its single-instance or multi-instance IP cores on a Xilinx SoC FPGA. This service leverages Xilinx's Vivado design suite software. Although the following example is based on a Xilinx FPGA and Vivado, Sital can perform similar integration for SoC FPGAs from Intel/Altera, Microsemi, Lattice or others using their respective design software suites.

Figure 1 provides an example of Sital's SVIVADO integration. As shown, the hardware consists of a Xilinx FPGA development board and a Sital BRD1553XVR-P 1553 transceiver/transformer board. The BRD1553XVR-P includes a PMOD connector interfacing the digital transceiver signals from the FPGA development board, a dual Sital transceiver and transformers and a pair of triax connectors for the MIL-STD-1553 bus signals.

Sital can integrate one of its single-instance or multi-instance 1553 IP cores on an FPGA. In the example of Figure 1, Sital integrates two of its BRM1553D MIL-STD-1553 IP cores on to a Xilinx Zynq Ultrascale FPGA. As shown, this includes interfacing the BRM1553D IP core to a Cortex A53 processor over the on-chip AXI bus. This includes interrupt logic between the BRM1553D and the on-chip processor.

The SVIVADO integration also includes the embedded software for accessing and controlling the BRM1553 IP core. As shown in the example of Figure 1, this software stack includes the BRM1553's API/library along with the low-level driver for accessing the BRM1553's memory and registers over AXI bus and servicing interrupts. As shown, the driver is designed for running under the PetaLinux real time operating system.



**Figure 1. SVIVADO Integration Example**

## SVIVADO Deliverables

Sital's deliverables for its SVAVDO integration packages include:

- **BRD1553XVR-P Transceiver/Transformer Board:** MIL-STD-1553B/1760 daughter board with PMOD interface (to Hosting Board) and front end triax connectors. Includes Sital MIL-STD-1553B/1760 transceivers and transformers.
- **BRM1553D MIL-STD-1553 IP Core:** MIL-STD-1553B/1760 FPGA IP Core (BRM1553D), pre-configured to support the AXI bus architecture back-end and the PMOD front-end.
- **Device Drivers:** Low latency AXI bus device drivers to control the BRM1553D FPGA IP, with support for either PetaLinux, VxWorks or "bare metal" (no operating systems) environments.
- **API/library Software:** DDC compatible API/library, written in ANSI C, fully verified and tested
- **Sample Application:** Skeleton ANSI C applications for BC/RT/MT use cases, providing a walk-through of how the API is leveraged to a working flow for all types of application modes.
- **VIVADO Project Files:** Xilinx VIVADO IDE project files for a rapid deployment on Xilinx designs.
- **Test Scripts:** Out-of-the-box testing and validation scripts for the FPGA IP to ensure it is loaded correctly and its pinout is fully functional.
- **Documentation:** Fully documented API user manual, quick start guide, HSID (Hardware Software Interface Document) and software source code.