OCTAVA™ - BC MODE

MIL-STD-1553 BUS CONTROLLER

PIN-TO-PIN REPLACEMENT AND SW DRIVER COMPATIBLE WITH DDC® ENHANCED MINIACE®

USER'S MANUAL FOR:

OCT-61588, OCT-61688 & OCT-61689

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1 INTRODUCTION

1.1 ABOUT THIS MANUAL

This document is the user's manual for OCTAVA™ devices OCT-61588, OCT-61688 and OCT-61689 family. These components are Pin-to-Pin replacement for DDC MiniACE components with 72 pins Gull-Lead package.

The OCT-61588, OCT-61688 and OCT-61689 device is a 1553 BC, RT and MT with 4k or 64 K Word of memory. This manual covers the Bus Controller (BC) part of these devices.

In order to reduce the complexity of this manual, it is split from the manual of the Remote Terminal (RT and Monitor Terminal (MT), even though in some configurations of the devices, the BC, RT and MT are packed together as a single component.

The OCTAVA™ device supports all three modes – BC, RT and MT. The software can enable either BC or an RT-MT combination, but cannot operate BC with RT or MT at the same time.

As a consequence of this selection, this separate BC document describes only BC settings. A typical Software user would either use this document for BC development OR use the RT+MT document for RT/MT development OR use both documents.

It should be noted that both the BC and RT/MT modes access the same registers and same memory element in hardware, so a careful study of both documents is required if BC and RT/MT modes of operation is required for the same device.

Note:
Please note that it is assumed that the user of this manual is knowledgeable about the DDC MiniACE and Enhanced MiniACE components, and their software interface. It is also assumed that the user of this manual has knowledge of Mil-Std-1553 protocol.

1.2 ABOUT OCTAVA™

1.2.1 GENERAL DESCRIPTION

The OCTAVA™ family of Mil-Std-1553 devices integrate Mil-Std-1553B protocol engine, a dual 5-volt transceiver, memory management, processor interface logic, and 4K or 64K words of RAM in a 72 Pin Plastic Quad Flat Pack (PQFP) package.

The OCTAVA™ (OCT-XXXXX) devices are pin-to-pin replacement devices for the respective DDC® BU-XXXXX devices. These replacements offer software and electrical compatible solution. A board designed to operate with the DDC® BU-65178, BU-61588, BU-65179, BU-61688 and BU-61689 can work seamlessly with OCT-65178, OCT-61588, OCT-65179, OCT-61688 and OCT-61689 respectively without hardware or software changes.

Please note that the OCTAVA™ core does not implement all of DDC's mini-ACE features, but rather the features which are used for the application. In most designs only a very small set of features are used from the DDC's interface. These features are implemented in the core.

This document describes the parts that are implemented. If there is a feature that is required by your software, but is not supported by OCTAVA™, then please contact Sital Technology.

The OCTAVA™ components were validated to meet the MIL-STD-1553B Notice 2 Remote Terminal Validation test plan, thus reliving the user from mastering the standard.

In some configurations the OCT-61588, OCT-61688 and OCT-61689 also work as a 1553 Remote Terminal or Monitor. Please refer to "OCTAVA™ RT & MT Users manual" for details on the RT and MT operation.

1.2.2 PRODUCTS SELECTION

The following table shows the different models of OCTAVA™ and the functionality:

Device Number	Functionality	Clock Frequency	RAM (16 bits)
OCT-65178	RT Only	16/12 MHz	4K RAM
OCT-61588	BC/RT/MT	16/12 MHz	4K RAM
OCT-65179	RT/RT_BOOT	10/12/16/20 MHz	4K RAM
OCT-61688	BC/RT/MT	12/16 MHz	64K RAM
OCT-61689	BC/RT/MT	10/20 MHz	64K RAM

1.2.3 BACK-END INTERFACE

The OCTAVA™ family contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The memory management scheme for RT mode provides three data structures for buffering incoming and outgoing data. Combined with the OCTAVA's extensive interrupt capability, these structures serve to ensure data consistency while off-loading the host processor. The OCTAVA™ devices can optionally boot-up as a RT with the Busy bit set for 1760 applications. The OCTAVA™ BC mode implements several features aimed at providing an efficient real-time software interface to the host processor including automatic retries, programmable inter-message gap times or message rate, automatic frame repetition, and flexible interrupt generation.

1.2.4 OCTAVA™ KEY FEATURES

- Fully integrated MIL-STD-1553B Notice 2 compliant terminals.
- Second source for DDC® MiniACE® devices.
- 5V or 3.3V operation.
- Flexible Processor/Memory interface.
- Bootable RT option required for MIL-STD-1760.
- Very fast access 4Kx16 or 64Kx16 Shared RAM.
- Automatic BC Retries
- Programmable BC Gap Times
- Programmable BC Message Rate
- Programmable Illegalization
- Simultaneous RT/MT Mode
- Operates from 10, 12, 16 or 20 Mhz.
- 72 Pins PQFP One-Square-Inch Package

1.4 TERMS USED IN THIS DOCUMENT

- Remote Terminal (RT) – The part of the FPGA that manages the 1553 communications and implemented by the core.
- SubSystem – The whole box that connects to the MIL-STD-1553 bus that contains the FPGA – part of it is the Remote Terminal.
- Host – the CPU running the SubSystem and managing the device interface.
- FPGA – Programmable device that contains the 1553 core and user logic and is part of the Subsystem.
- 1553 Core – Supplied logic circuit that interfaces to MIL-STD-1553 bus.
- ICD - Interface Control Document.
- BC – Bus controller.
- TA – Terminal Address of the command / status words. Bits 11 to 15.
- SA – Sub Address of the command word. Bits 5 to 9.
- WC – Word count field of command. Bits 0 to 4.
- Muxbus – Time multiplexed bus known as the MIL-STD-1553B Notice 2 bus.
- SW – software.
- BCST – Broadcast command.
- TX – Transmit.
- RX – Receive.
- SACW – The Sub-address control word.
- LUT – Look up Table.

2 HARDWARE INTERFACE

2.1 DEVICE SPECIFICATIONS

2.1.1 OPERATING CONDITIONS

Parameter	Symbol	Min	Typ.	Max	Units
Power supply					
Supply voltage	Vcc, Vcc1, Vcc2	4.7		5.5	Volts
Standby current	Iccstby				mA
100% XMT current	Icc100			675	mA
Logic					
High level input voltage	V_{IH}	Vcc x 0.7		6.5	Volts
Low level input voltage	V_{IL}		Vcc x 0.3		Volts
Input / Output voltage (active)	$V_{I/O}$	0		Vcc	Volts
Input / Output voltage (3-State)	$V_{I/O}$	0		5.5	Volts
High level output current	I_{OH}			-32	mA
Low level output current	I_{OL}			32	mA
Input transition rise or fall rate	Δt / Δv			5	ns/V
1553 bus					
1553 Bus level	Vpp	7.1			Volts
1553 Stub level	Vpp	20		27	Volts
1553 message timing:					
Completion of CPU Write (BC Start)- to-Start of Next Message			2.5		µS
BC Intermessage Gap		7	9.5		µS
BC/RT/MT Response Timeout				25	µS
Transmitter Watchdog Timeout				770	µS
Operating free-air temperature	T_A	-40		+85	^{0}C

2.1.2 OPERATING CONDITIONS (3.3V LOGIC, 5V TRANSCEIVER)

TBD

2.1.3 ABSOLUTE MAXIMUM RATING

Parameter	Min	Typ	Max	Units
Supply Voltage	-0.5	5.0	6.5	Volts
Logic				
V_I – Input Voltage Range	-0.5		6.5	Volts
V_O – Voltage range applied to any output in the high impedance state	-0.5		6.5	Volts
V_O – Voltage range applied to any output in the high or low state	-0.5		VCC+0.5	Volts
I_{IK} – Input clamp current when V_I<0			-50	mA
I_{OK} – Input clamp current when V_O<0			-50	mA
I_{OK} – Continuous output current			±50	mA
Power dissipation	0.2	0.4	0.75	Watts
Supply current (all pins)	0.2	0.4	0.7	Amperes
Operation temperature	-40		+85	Degrees ^{0}C

2.2 INTERFACE SIGNALS

The following figure shows the pinout of the OCTAVA™ component:

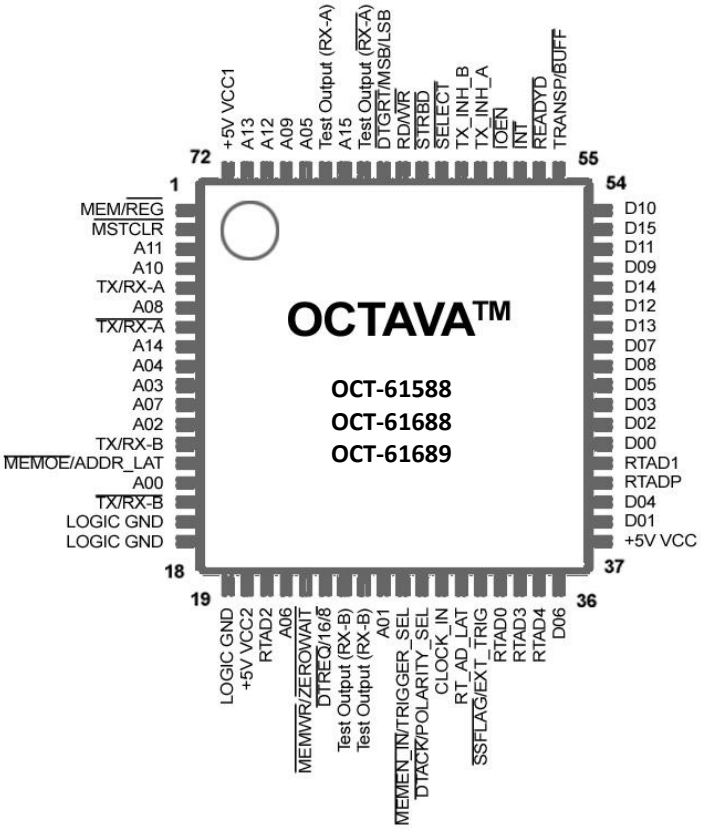

Figure 1: OCTAVA™ Pinout

2.3 PIN DESCRIPTIONS

Name	Function	Description
MEM/$\overline{\text{REG}}$	Input	Address space selection. When this line is logic '1' then the address lines correspond to the internal memory space, when '0' then address lines correspond to the internal registers.
$\overline{\text{MSTCLR}}$	Input	Master Clear. When set to low, this signal resets the OCTAVA™ device. Memory content is not reset.
A14-A15	Inputs	In OCT-61688 and OCT-61689 used as address lines A14-A15. In OCT-65179 used as Clock selection: "00" – 20 Mhz (10Mhz not supported – see note 2). "01" – 20 Mhz. "10" – 12 Mhz. "11" – 16 Mhz.
A13	Input	In OCT-61688 and OCT-61689 used as Address line 13. In OCT-65179 this pin is not used.
A12	Input	In OCT-61688 and OCT-61689 used as Address line 12. In OCT-65179 used as boot up mode selector. Logic '1' – boots up as BC. Logic '0' – boots up as RT with busy bit set (MIL-STD-1760).
A00-A11	Inputs	Address inputs 0 to 11.
TX/RX-A,$\overline{\text{TX/RX-A}}$	Input/Output	Positive and negative polarity of 1553 signals for Bus A. These signals should be connected to a Mil-Std-1553 or Mil-Std-1760 transformer.
TX/RX-B,$\overline{\text{TX/RX-B}}$	Input/Output	Positive and negative polarity of 1553 signals for Bus B. These signals should be connected to a Mil-Std-1553 or Mil-Std-1760 transformer.
ADDR_LAT/ MEMOE	Input	During I/O operation, address is latched on rising edge. When this line is logic '1' then the data from the latched address will appear on the Data bus. MemOE option is not used.
LOGIC GND	Power	Power supply Ground, 0V.
+5V VCC, VCC2	Power	Power supply input, 5Vdc ±5%
RTAD0-RTAD4	Inputs	RT address. These pins determine the address of the RT on the 1553 bus.
RT_AD_LAT	Input	RT Address Latch. RT address is latched on rising edge.
$\overline{\text{MEMWR}}$/ ZEROWAIT	Input	Should be tied to high. Only non-zero wait-state supported by OCTAVA™ (see note 3).
$\overline{\text{DTREQ}}$/16/$\overline{8}$	Input	This input is ignored. OCTAVA™ works in 16-bit bus width only. This line should be tied to high (note 1).
Test Output (RX-A) Test Output (RX-A)	Outputs	Positive and negative polarity of 1553 signals for Bus A, for testing purposes.
Test Output (RX-B) Test Output (RX-B)	Outputs	Positive and negative polarity of 1553 signals for Bus B, for testing purposes.

TRIGGER_SEL/ MEMEN-IN	Input	This input is ignored. OCTAVA™ works in 16 bit bus width buffered mode. This line can be tied to high or low (note 1).
POLARITY_SEL/ DTACK	Input	Selects the polarity of the RD/WR signal. High - Read data with RD/WR = '1', write when '0'. Low - Read data with RD/WR = '0', write when '1'.
CLOCK_IN	Input	Clock input. Clock can be 12MHz, 16MHz or 20MHz, as selected by A14 and A15 in OCT-65178, or clock configuration register in OCT-65688
$\overline{\text{SSFLAG}}$/EXT_TRIG	Input	RT mode – When low sets the subsystem flag bit in the status word response. BC mode – A rising edge on this signal triggers a frame if external trigger enabled in configuration register #1.
D00-D15	Input/Output	Data bus signals.
TRANSP/$\overline{\text{BUFF}}$	Input	This signal should be connected to Ground. OCTAVA™ only works in buffered mode (note 1).
$\overline{\text{READYD}}$	Output	When non-zero wait-state mode, logic '0' on this signal indicates to the host CPU that the read or write cycle is done. Zero wait state mode is not supported by OCTAVA™ (note 3).
$\overline{\text{IOEN}}$	Output	I/O Enable – This signal is low when OCTAVA™ is performing the requested host bus cycle. Normally this signal should not be used.
TX_INH_A	Input	When high – Transmission is inhibited for 1553 Bus A.
TX_INH_B	Input	When high – Transmission is inhibited for 1553 Bus B.
$\overline{\text{SELECT}}$	Input	Active low chip select for the OCTAVA™ device for memory and register access.
$\overline{\text{STRBD}}$	Input	Data strobe. Should be held low by the host during a read or write cycle.
RD/$\overline{\text{WR}}$	Input	During Read or Write cycle to the device, when this line is logic '1' then this is a read cycle. If this line is logic '0' then data from the data bus is written to the device.
$\overline{\text{DTGRT}}$/MSB/LSB	Input	Not used by OCTAVA™, may tied high, low or left open (note 1).

Notes:

1. OCTAVA™ supports DDC® BU-65178, BU-61588, BU-65179, BU-61688 and BU-61689 pin-out and functionality. It does not support 8 bits operation and "transparent mode".
2. OCTAVA™ supports 12MHz, 16MHz and 20MHz clock operation. In OCT-61688 clock selection is set by register.
3. All models with 4K Memory support zero wait-states. OCT-61688 and OCT-61689 support only non-zero wait-states mode.

2.4 INTERFACE TO THE 1553 BUS

The OCTAVA™ components require a coupling transformer with a turns ratio of 1: 2.5 for Direct Coupling, and a turns ratio of 1: 1.79 for Transformer Coupling to the Mil- Std- 1553 Bus.

The center tap on the OCTAVA™ side of the coupling transformer must be grounded. The center tap on the bus side of the coupling transformer should be left floating.

The following figure shows a typical transformer connection.

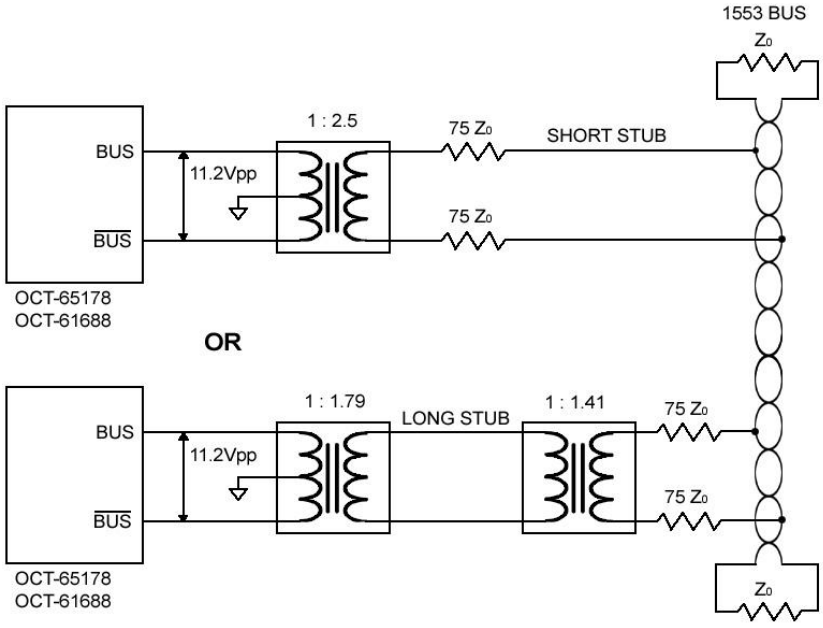

Figure 2: OCTAVA™ transformer connection

2.5 BACKEND INTERFACE

Read or Write cycles with OCTAVA™ require data, address and control signals. Since it is assumed that OCTAVA™ does not necessarily uses the same clock as the host CPU, then special care is taken in order to assure data integrity.

2.5.1 WRITE CYCLE

The following figure illustrates a write cycle. This cycle is identical between memory and registers write.

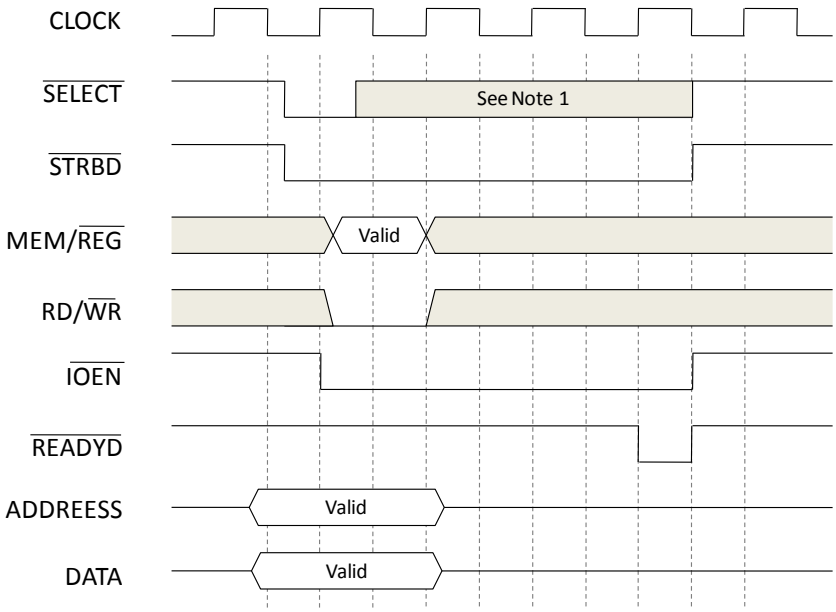

Figure 3: Write Cycle

Notes:

1. In most cases SELECT and STRB are tied together.
2. POLARITY_SEL is assumed to be high. This affects the polarity of RD/WR.
3. MEM/REG is high for memory access and low for registers access.
4. MEM/REG and RD/WR are latched internally on the first falling edge of CLOCK, after SELECT and STRB are low.
5. ADDRESS is latched internally on the first rising edge after IOEN goes low.
6. DATA is latched internally on the first rising edge after IOEN goes low.

2.5.2 READ AND INTERRUPT CYCLES

The following figure illustrates a read cycle. This cycle is identical between memory and registers read.

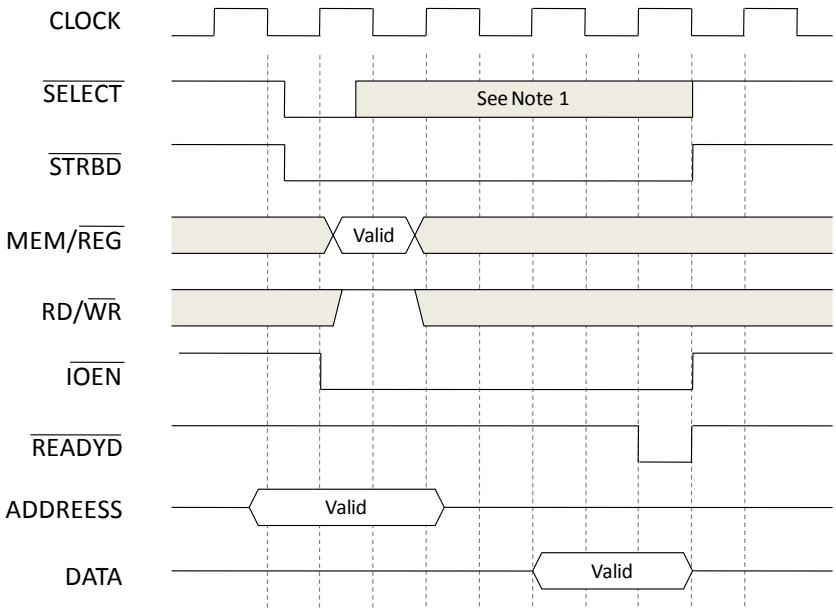

Figure 4: Read Cycle

Notes:

1. In most cases SELECT and STRB are tied together.
2. POLARITY_SEL is assumed to be high. This affects the polarity of RD/WR.
3. MEM/REG is high for memory access and low for registers access.
4. MEM/REG and RD/WR are latched internally on the first falling edge of CLOCK, after SELECT and STRB are low.
5. ADDRESS is latched internally on the first rising edge after IOEN goes low.
6. Data may be valid on rising edge after ADDRESS is latched internally.

3 BUS CONTROLLER INTRODUCTION

3.1 OVERVIEW

The 1553 Bus Controller (BC) allows a subsystem to control the 1553 bus. Control is achieved by sending instructions to RTs connected to the bus. Each command either instructs the RT to transmit words, receive words from the BC or perform some special actions, known as mode commands.

The Host programs the device with the relevant messages data alongside some configuration registers. Many such messages are loaded into the shared memory by the host.

The Host normally wants to attend the device only once every slice time. This slice time is referred to as a frame. During a frame, many messages are transferred between the BC and the RTs and between the RTs themselves (RT to RT commands). The Host needs to load the device with a complete set of messages for the entire frame.

When all commands per frame have been loaded to the device's memory, the host initiates the frame. From this point the device will sequence the messages one after the other until all messages are done. No need for Host intervention is required during the frame run.

When the frame is finished, all data received is waiting in the device's memory for Host analysis.

Typically for real-time operation, frames would be initiated every 20 ms.

The device can be programmed to repeat its frames automatically, thus off loading the Host from sequencing the 1553 bus even further.

The Enhanced Mini-Ace BC chip provided by DDC can work in two different modes. The legacy BC and Enhanced BC. The BC core and this document support only the legacy BC (R18B15='0') in Enhanced mode (R07B15='1') and Enhanced BC control word (R08B12='1').

3.2 BLOCK DIAGRAM

The host processor controlling the core accesses the memory and registers located in the host interface block. By setting the values of the configuration registers and setting up the transmission stack in memory, the host processor defines which commands would be transmitted to the 1553 bus.

The block diagram of OCTAVA™ BC Mode is illustrated below:

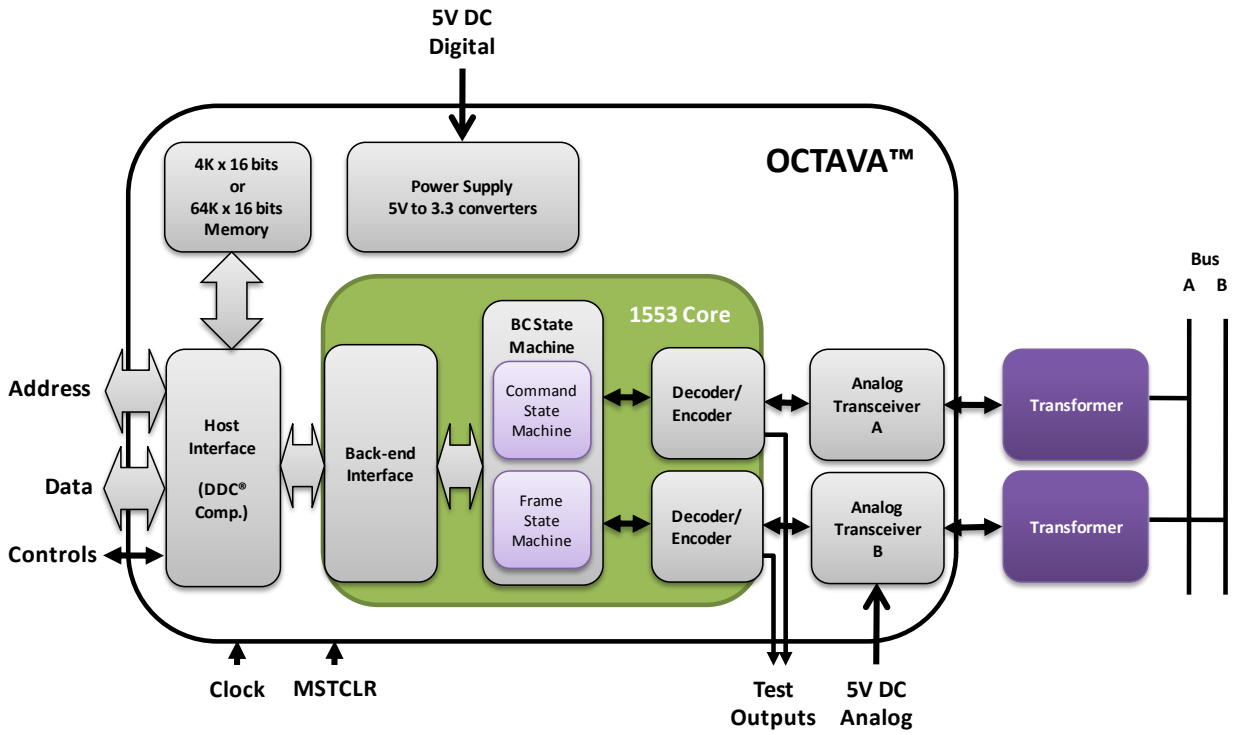

Figure 5: OCTAVA™ Block Diagram – BC Mode

When transmission is initiated the frame state machine manages the sequencing of a whole frame of messages as defined by the configuration registers and fixed memory locations in the memory.

The whole frame is composed of a set of individual messages being transmitted and managed over the 1553 bus one after the other. The host also points the beginning first message in memory and defines how many messages to transact through 2 fixed location memory words.

When all data has been loaded, and the state machines are idle, the host sends a START command. As a response, the frame state machine starts the frame transmission. The frame state machine fetches the messages from memory and forwards the requested message information to the command state machine which in turn sequences the command data and status words for a complete legal 1553 message.

When the message is complete the frame state machine accesses the next command, and so on until all messages have been completed.

The command state machine either transmits words through the encoders or receives RT responses through the decoders. The encoders and decoders interface between the core's 16 bits parallel internal buses and the MuxBus serial bus.

3.3 BUS CONTROLLER OPERATION MODES

3.3.1 BASE OPERATION

The host manages the 1553 bus through the shared memory and several registers. The host should load these registers and memory prior the START command, and then analyze the results in memory after the messages transactions have been finished.

The memory data defines which messages need be transmitted and when. The host stores the messages table in the stack area of the memory.

The stack is located in the first 256 words (512 bytes) of the memory space. The stack defines 64 blocks of 4-word message descriptors. Each message descriptor describes a message that needs to be transmitted and managed by the core.

The typical BC operation is organized in frames. Each frame includes several messages. Once the BC is triggered, the core's internal state machines start to manage each message, one after the other until finished.

When the BC core is triggered by the START command (R03B02) it looks for two memory locations in the shared memory.

Address M0100 is initially set by the host and points to the first stack entry from which the core starts to run. This address is in the range of 0 to 252. The 2 LSBs are ignored because each message occupies 4 memory words. The internal state machine automatically rolls over from M00FF to M0000 when reached the end of the stack.

Using address M0101 the host defines the number of stack entries that the core is required to run until it stops the frame. NOTE that the host should load the 1's compliment of the number of messages to run. If only one message in frame than load 0xFFFE.

3.3.2 MULTI FRAME SETUP

In most avionics systems, not all messages are transmitted every frame. There are messages that need to be transmitted once every 20ms, others every 40ms, 80ms…

The above mechanism supports this type of management. The host should load the stack with the messages for the first frame, then the messages for the second frame, and so on until all frame types are described in stack. Then, before the start of each frame, the host should write the stack new start point to address 0x0100, and define its length in 0x0101, and then order the START command (R03B01).

3.3.3 AUTO-REPEAT MODE

In order to off load the host from the burden of initializing each frame with the START command, the core supports the auto-repeat mode. By defining the frame length (Register 0D) and enabling a configuration register, the core would restart the same frame it finished all over again automatically. In order to work in auto repeat mode, the

host should set the appropriate configuration register and load M0102 with the repeated start point, and M0103 with the repeated length. The core will read these values if auto repeat is on (R01B08) and copy to M0100 and M0101 and update them continuously during the frame. When the frame is finished, the core will wait for the frame counter zero (if zero occurred BEFORE the frame has been completed, the core will restart the frame with standard gap time after the last message. This can happen if many retries have happened during the frame).

3.3.4 MULTI-FRAME & AUTO-REPEAT

If multi frame mode is required and also auto repeat is required then the above multi frame setup requires different settings before each frame, which cannot be accomplished by the host in auto repeat mode.

For this challenge, a programmable message-to-message gap can be enabled. Each stack entry's third word defines the number of microseconds from the start of this message until the start of the next message. Up to 65.5 ms can be programmed with the third word.

The host should load all of the messages of the first frame, consecutively load all messages of the second frame, and so on. The groups of messages that define a frame in stack are called **minor frames**. All of the minor frames together, from the first message of the first frame until the last message of the last frame, are called the **major frame**.

If each message in the minor frame has a pre defined gap time, the total minor frame transmission period can be summed, and the gap time of the last message in the minor frame should be programmed to compensate for the gap to the next frame.

For example, if frames are separated by 20ms, and a frame is composed of 5 messages, each programmed to 1 ms gap, then the total message activity will take 5 ms. In this case the gap time to the fifth message should be set to 15 ms.

Calculating the gap time for each message requires 1553 know-how as to how each message is spread over time. Rule of the thumb would be = (number of data words + 3) * 20 us. For RT 2 RT format = (number of data words + 6) * 20 us (where 3 and 6 are the number of extra control words per message).

The frame counter should be loaded with major frame time. The major frame time is sum of all minor frames.

3.3.5 RETRY

Sometimes in life, things don't work, they just don't. There are sometimes failures. This also happens in 1553 serial communication during operation. In this case the core allows for retries. Retry can be enabled globally through the configuration registers (R01B04) and if enabled, each message can be set to retry on failure using the message control word.

Retry can also be set to perform on the same bus or the opposite bus from the failure.

If the optional first retry fails, an optional second retry can be initiated using the message control word.

3.3.6 STOP ON ERROR

When things do go wrong and messages fail, the core can be programmed to stop.

The core state machine can be stopped at the end of a failed message, or at the end of the frame that contained a failed message.

A failed message is a message that even optional retries didn't solve the error. If retry passes, the message is not considered a failure.

3.3.7 STOP ON STATUS BITS

The core can also be programmed to stop its frame or stop frames in auto repeat mode if bits of the RT's status word are not as expected. Each of these bits can be masked, so even if the bit is set, it is not considered as a reason for stopping the frame.

The broadcast bit has a special treatment. It could either be masked OR it could be compared to either '1' or '0'.

4 PROGRAMMING AND SETUP

4.1 REGISTERS

There are several registers mapped to the register section (when MEM_REG signal is kept low) during a read or write operation.

The following section describes the registers and the operational bits of these registers.

Note:
If a bit is defined as read only, then the core acts according to the specified level, and the read operation is available for software compatibility with DDC reasons. However, these bits may be written with values which will be ignored by the core.
If the bit is Write/Read, then the default value is as defined but could be changed to desired level for the required operation.

Note for the way this section is written:
If a reference is made to a particular **register** and a specific bit the notation is R01B12 for Register 01 bit 12.
If a reference is made to a particular **memory** location the notation is M0100 for memory address 0x100.

4.2 REGISTERS MAP

The software interface of the core to the host processor consists of 20 internal operational registers for normal operation. These registers determine the device configuration, modes of operation, memory structure, interrupt control and status, etc.

The address mapping for the registers is detailed in the following table:

Address Lines					Register Description (Read/Write)
A4	A3	A2	A1	A0	
0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	1	Configuration Register #1 (RD/WR)
0	0	0	1	0	Configuration Register #2 (RD/WR)
0	0	0	1	1	Start/Reset Register (WR)
0	0	0	1	1	Stack Pointer Register (RD)
0	0	1	0	0	RT Subaddress Control Word Register (RD) – Not used in BC mode
0	0	1	0	1	Time Tag Register (RD/WR)
0	0	1	1	0	Interrupt Status Register #1(RD)
0	0	1	1	1	Configuration Register #3 (RD/WR)
0	1	0	0	0	Configuration Register #4 (RD/WR)
0	1	0	0	1	Configuration Register #5 (RD/WR) – Not used in BC mode
0	1	0	1	0	(RD) – all '0'
0	1	0	1	1	BC Frame Timing Remaining (RD)
0	1	1	0	0	BC Message Timing Remaining (RD)
0	1	1	0	1	BC Frame Time Register (WR)
0	1	1	1	0	RT Status Word Register (RD) – Not used in BC mode
0	1	1	1	1	RT BIT Word Register (RD)
1	0	0	0	0	Not implemented
1	0	0	0	1	Not implemented
1	0	0	1	0	Not implemented
1	0	0	1	1	Not implemented
1	0	1	0	0	Not implemented
1	0	1	0	1	Not implemented
1	0	1	1	0	Not implemented
1	0	1	1	1	Not implemented
1	1	0	0	0	Configuration Register #6 (RD/WR) – Not Used
1	1	0	0	1	(RD) – all '0'
1	1	0	1	0	Front End version of Core (RD)
1	1	0	1	1	Back End version of Core (RD)
1	1	0	1	1	Not relevant for RT – see BC mode manual for details
1	1	1	0	0	BIT Test Status Register (RD)
1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
1	1	1	1	0	Interrupt Status Register #2 (RD)
1	1	1	1	1	Not relevant for RT – see BC mode manual for details

Note:
Not all of the bits of the DDC MiniACE registers are implemented. Please see "1553 Core compatibility" document for details on all differences between the 1553 Core and DDC MiniACE and Enhanced MiniACE.

4.3 REGISTER'S SHORT FORM LOOK UP TABLE

Reg / Bit	Int Reg **0x0**	Configuration 1 **0x1**	Configuration 2 **0x2**	Start Reset **0x3**	Time **0x5**	INT Status **0x6**	Conf 3 **0x7**	Configuration 4 **0x8**	Frame **0xD**
15		0 for BC	1 (enhanced Int)		Time Tag Value	OR of below	'1'		Frame Length LSB is 100 us
14							Stack Size		
13	Tx Timeout					Tx Timeout			
12	Stack Rollover	Error Stop EOM				Stack Rollover		'1'	
11		Error Stop EOF						Mask BCST	
10		Sts Stop EOM	No 256 Boundaries						
9	Mem Protect	Sts Stop EOF	"000" preset to 64 us Time Tag Step			Mem Protect		Retry STS	
8	BC Retry	Auto Repeat				BC Retry		1st Retry Opposite	
7	RT Addr Parity	Ext Trigger				RT Addr Parity		2nd Retry Opposite	
6	Time Rollover	Int Trigger		Stop EOM		Time Rollover		ME valid	
5		Gap Enable	Sync Internal	Stop EOF				Busy Valid	
4	Filtered EOM	Retry Enable	Clear INTv on Read			Filtered EOM			
3	EOF	Retry Twice	1 – Level INT	Reset Time		EOF			
2	1553 Error	BC is IDLE		Reset INTv		1553 Error			
1	RT statused	Frame Active		Start BC		RT statused			
0	EOM	Message Active		SW reset		EOM			
Init value	0x0000	0x0000	0x9C73	Reads Stack point		0x0000	0x8000	0x1060	

4.3.1 INTERRUPT ENABLE REGISTER #1 ADDRESS 0X0

If the Host enables one of the bits below by setting its value to '1', and the specified event occurs, an interrupt will be generated to the Host CPU.

Bit number	Read/ Write/ Default	What event triggers the interrupt when enabled by '1'.
13	R/W/0	Transmitter timeout occurred
12	R/W/0	Stack Rollover occurred
9	R/W/0	Memory protection fault **
8	R/W/0	BC Retry – following incorrect RT response has been initiated.
7	R/W/0	RT Address parity error found
6	R/W/0	Time tag counter rollover
4	R/W/0	BC End Of Message.
3	R/W/0	BC End Of Frame.
2	R/W/0	1553 message error occurred.
1	R/W/0	Wrong RT status or unexpected status bits set in status respond.
0	R/W/0	End Of Message.

*All other bits are not used and will be read as zero. Default Value: 0x0000 – all events masked.

** This bit is used in DDC Mini-ACE as memory handshake error. Since this cannot occur with the core, bit #9 is used for data protection. When Data pointer points to a non data block area (M0000 to M0103) due to wrong memory setup by the host, the core detects that, and asserts bit 9 of the interrupt status register interrupt to '1'. If this bit is not masked than an interrupt will occur.

Memory overrun is not prevented in BC mode, only an interrupt is set.

4.3.2 CONFIGURATION REGISTER #1 ADDRESS 0X1

This configuration register works in BC function if bit 15 is '0'.

This configuration register only works in "RT without Alternate Status" mode if bit 15 is '1'. For RT/MT register description and initial values please refer to RT+MT document.

Bit number	Read/ Write/ Default	Description
15	R/W/1	'0' For legacy BC. All default values below are in BC mode. '1' For Enhanced RT (see RT/MT documentation) following values assume this bit is set to '0'
14	Assumed '0'	'0' is preset for this bit.
13	Assumed '0'	'0' always area A.
12	R/W/0	'1' – Stop at end of Message error. If optional retry succeeded => messages continue!
11	R/W/0	'1' – Stop at end of frame if error. If optional retry succeeded => frames continue!
10	R/W/0	'1' – Stop messages if unexpected, non-masked status bits are set. If optional retry succeeded => messages continue!
9	R/W/0	'1' – Don't process additional frames if message unexpected, non-masked status bits are set and auto frame enabled. If optional retry succeeded => frames continue!
8	R/W/0	'1' – Auto Frame Repeat. Will start next frame if none of the problems in bits 9-12 caused a halt. Refer to setting up auto repeat presets. Trigger first frame with START (R03B01). '0' – Host has to trigger every frame with START.
7	R/W/0	'1' – External trigger mode – sensitive to rising edge. (***** The external trigger works on rising edge? Or this bit, once? ****) '0' – External trigger disable.
6	R/W/0	'1' – Internal frame counter (64K steps of 100 us) re-trigger the frame in case auto frame repeat is enabled (bit 8). '0' – Internal trigger disable.
5	R/W/0	'1' – Message gap timer enable. If enable will start next message after gap*1us. Gap is defined in 3rd word in BC message block descriptor in stack. '0' – Message gap set to default (~10 us).
4	R/W/0	'1' – Global Retry enable. If enabled, each message can be enabled for retry with its BC control word bit 8.
3	R/W/0	'1' – Retry twice after 2 failures. '0' – Retry only once after failure.
2	Read	'1' – BC state machine has been started, and has not finished its messages transactions. In Auto repeat mode this signal will stay high until halted by host or error. '0' – BC is idle (after frame finished or "stop on error").
1	Read	'1' – bus active – from start of first message in frame till end of last message in frame.
0	Read	'1' - Message active – from start till end of message.

4.3.3 CONFIGURATION REGISTER #2 ADDRESS 0X2

Bit number	Read/ Write/ Default	Description
15	Assumed '1'	'1' – Enhanced Interrupts mode enabled. Interrupt status register will set its bit flags high if condition occur even if it is masked by the interrupt enable register. An interrupt will be generated if a bit is set and also enabled.
14	Assumed '0'	'0' – No Memory Parity bit.
13	Assumed '0'	RT mode.
12	Assumed '1'	RT mode.
11	Assumed '1'	RT mode.
10	Assumed '1'	256-word boundaries disable. '0' for RT mode. '1' in BC mode.
9..7	R/W/'000'	Time Tag resolution: "000" – 64 usec, "001"– 32 usec, "010"– 16 usec, "011"– 8 usec, "100"- 4 usec, "101"- 2 usec, any other – 64 usec.
6	Assumed '1'	RT mode.
5	Assumed '1'	'1' – in BC mode – transmits the internal time tag word in "synchronize with data" mode command.
4	Assumed '1'	'1' – Auto clear of interrupt status registers #1 as a result of CPU reading its value.
3	R/W/0	'0' – generates a 500ns low pulse on the INTn signal. '1' – Level mode. INTn stays low until the host reads interrupt status register.
2	R/W/0	RT mode.
1	R/W/1	RT mode.
0	Assumed '1'	RT mode.

Default Value: RT mode 0x0000, BC mode 0x0000

4.3.4 START RESET REGISTER WRITING TO ADDRESS 0X3

This is a write only register. Reading back will return Stack Pointer Register (same as reading address 0x0100).

Bit number	Read/ Write/ Default	Description
10	Write	'1' clear self test register at address 0x1C.
9	Write	'1' initiate RAM self test.
7	Write	'1' initiate Protocol self test.
6	Write	'1' stop BC operation at end of message.
5	Write	'1' Stop BC operation at end of frame.
3	Write	'1' resets the Time Tag counter.
2	Write	'1' resets the interrupt. Resets the FF that latches the interrupt condition. If the condition for interrupt persists, the relevant FF would be set again until the condition for causing this interrupt is cleared. Reset of Interrupt Register #1.
1	Write	'1' BC START command. Starts the BC state machine.
0	Write	'1' Reset core. Reset all registers, FFs in core. Memories are not reset, and should be reset by CPU.

4.3.5 STACK POINTER REGISTER READING FROM ADDRESS 0X3

This is a read only register. Writing to it is explained above.

Bit number	Read/ Default	Description
15..0	Read 0x0	Copy of the Stack pointer value. After the EOM bit (15) is written to the first word of the stack entry, the stack pointer is incremented by 4. This pointer value can either be read from the memory in address 0x100, or from this register.

4.3.6 BC/RT SUB-ADDRESS CONTROL WORD. ADDRESS 0X4

This register is not in use in BC mode.

4.3.7 TIME TAG REGISTER – ADDRESS 0X5

The time tag counter can be reset by writing to this register value 0x0 or loaded to any other value by writing it here.

The time tag counter counts in clock steps of 64us.

The counter will rollover every 64us * 2^16.

The value of this counter is also reset by the hardware raw_reset line, or the software reset done by writing '1' to R03B00 or R03B03 register.

The value of the time tag counter is placed in the stack of each transmitted command. Please see "Stack contents" section for details.

The BC Host may write to this register any time.

When performing synchronize with data command, the time tag value can be sent instead of the data word in the stack memory. The BC control word bit 15 controls the source of this data word.

The best system synchronization would be achieved with Broadcast synchronize with data sent out by the BC every 64us * 2^16 = 194304.4 seconds.

Bit number	Read/ Write/ Default	Description
15..0	Read/Write 0x0	Read the Time Tag Counter. Write a new value to the time tag counter.

4.3.8 INTERRUPT STATUS REGISTER #1 ADDRESS 0X6

This register indicates the cause of an interrupt.

To reset this register either read it or write '1' to R03B02.

Bit number	Description
15	This bit is an OR of all interrupts bits of this register.
13	'1' – Transmitter fail safe timeout.
12	'1' – Stack Rollover has occurred
9	'1' – Data Pointer pointed to a protected area where data blocks should not be present. Data was not written and memory was not corrupted. (Handshake Error in DDC devices)
8	'1' - BC retry has occurred. Each message has a bit in status word in stack that indicates if retry was done.
7	'1' - RT Terminal Address Parity Error. RT mode.
6	'1' - Time Tag Rollover from 0xFFFF to 0x0000.
4	'1' – Message was sent. This interrupt can be enabled or not for each message with BC control word bit 4.
3	'1' – BC has reached end of frame.
2	'1' – RT has not replied OR replied with error OR loop-back error of transmitted words.
1	'1' – Wrong RT address response or one of the (non BCST) status word bits were set high. BCST bit sets this bit high if configurations register 4 bit number 11 is set low (compare mode) AND the BCST bit is different from the BC control word of the message bit #5.
0	'1' – End of message has occurred.

*All other bits are not used and will be read as zero.

Default Value: 0x0000

4.3.9 CONFIGURATION REGISTER #3 ADDRESS 0X7

Bit #	Read/Write/ Default	Description
15	Assumed '1'	'1' always in Enhanced mode.
14..13	Write/Read/'00'	BC stack size selected as follows: (bits 14,13) "00"- 256 words / 64 messages "01"- 512 words / 128 messages "10"- 1024 words / 256 messages "11"- 2048 words / 512 messages See note 1 below.

Note 1: The core will update the 8 LSBs of the stack pointer in "00" mode, 9 LSBs in "01" mode, 10 LSBs in "10" mode and 11 LSBs in "11" mode. The host defines the Stack pointer, and the core will affect only the relevant lower bits.

4.3.10 CONFIGURATION REGISTER #4 ADDRESS 0X8

Bit number	Read/ Write/ default	Description
12	Assumed '1'	Expanded BC control word always on. All 15 bits of BC control word are functional.
11	R/W/0	Mask / Compare the BCST bit in returned status bit. ** '1' – Mask. The relevant bit in the BC control word operates as mask for the BCST bit of the received status. '0' – Compare. The relevant bit in the BC control word is compared with the BCST bit of the received status.
9	R/W/0	'0' – No retry if status bits that are not masked are set. '1' – Retry a message if retry enabled and one of the unmasked status bits are set high in the returned RT status word. BCST bit pass/fail has a special treatment as seen above in bit 11 setup.
8	R/W/0	'0' – First retry on same bus if message failed. '1' – First retry on opposite bus if message failed.
7	R/W/0	'0' – Second retry on same bus as original failed message. '1' – Second retry on opposite bus of original message.
6	Assumed '1'	An RT can respond to a transmit command with Message Error bit set followed by the data words OR without any data words (as in illegal command) and no format error is reported for either response. Both are valid responses.
5	Assumed '1'	An RT can respond to a transmit command with Busy bit set followed by the data words OR without any data words (as in busy RT state) and no format error is reported for either response. Both are valid responses.

*All other bits are not used and will be read as zero.

** Note that the BCST bit in the status return is only set by the RT in the proceeding message's status word after a broadcast message FOR a transmit status or transmit command mode commands. Otherwise the BCST bit should be '0'.

4.3.11 CONFIGURATION REGISTER #5 ADDRESS 0X9

This register should be ignored in BC mode.

This register is used in RT/ MT mode.

4.3.12 BC FRAME TIMING REMAINING ADDRESS 0XB

16 bits that define the number of 100us left until end of frame, or zero.

This is a count-down register that is read only.

4.3.13 BC MESSAGE TIMING REMAINING ADDRESS 0XC

16 bits that define the number of 1us left until the start of the next message, or zero.

The value is relevant only when this mode is enabled with the configuration registers.

This is a count-down register that is read only.

This register starts from the value of the 3rd word in the BC command descriptor in Stack.

4.3.14 BC FRAME TIME REGISTER ADDRESS 0XD

These 16 bits define the number of 100 us that is the frame length.

The frame length can be set from 100 us (0x0001) to 6.55 seconds (0xFFFF).

The running value can be read from register address 0xB.

4.3.15 FRONT END VERSION OF CORE REGISTER ADDRESS 0X1A

This register returns the revision of the front-end logic.

4.3.16 BACK END VERSION OF CORE REGISTER ADDRESS 0X1B

This register returns the revision of the back end logic.

4.3.17 SELF TEST STATUS REGISTER 0X1C

This register indicates the state of the internal protocol and RAM tests.

Writing to reset register at address 0x3 clears the content of this register.

Bit number	Description
15	Protocol Built-in-test complete
14	Protocol Built-in-test in progress, should be less than 2 ms.
13	Protocol Built-in-test passed
11	Protocol Built-in-test in progress or complete
7	RAM Built-in-test complete
6	RAM Built-in-test in progress, should be less than 2 ms.
5	RAM Built-in-test passed

After hardware power up, the core initiates the protocol test automatically. Allow 2 ms for this test to complete.

4.4 MEMORY

4.4.1 MEMORY MAPPING

The host should prepare the frames of messages in the memory prior to initiating the START command.

The following table suggests a memory mapping for the BC core.

Note that BC mode uses the same fixed addresses as the RT and MT, thus BC cannot operate in the same time RT/MT is used.

Hex Address	Description	Comments
0000 to 00FF	Stack	Initialized by host, Updated by core.
0100 (fixed)	Stack Pointer	Initialized by host, Updated by core.
0101 (fixed)	Frame length (1's complement)	Initialized by host, Updated by core.
0102 (fixed)	Initial Stack Pointer	Initialized by host. For Auto-repeat.
0103 (fixed)	Initial Frame length (1's complement)	Initialized by host. For Auto-repeat.
0108 to 012D	Message Block 0	
012E to 0153	Message Block 1	
:		
0ED6 to 0EFB	Message Block 93	

Shown for 4Kx16 memory array.

More memory can be loaded with additional Message Blocks.

If auto-repeat mode is ***not*** used please set:

1. The **Stack pointer** (M0100) points to the currently stack entry. The host sets the initial value prior to START command. After START command the core updates it constantly. The host should NOT change it after START but it could be read.

2. The **Frame Length** (M0101) is the number of stack entries (messages) that the host wants to transact. ***The one's compliment*** of the desired frame length should be loaded to this memory location. If 5 messages are required, load the value 0xFFFA to M0101.

If auto-repeat mode is used please set:

1. The **Initial Stack pointer** (M0102) points to the first stack entry. The host sets the initial value prior to START command. After START command the core updates the stack pointer (M0100) constantly. The host should NOT change it after START but it could be read.

2. The **Initial Frame Length** (M0103) is the number of stack entries (messages) that the host wants to transact. The one's compliment of the desired frame length should be loaded. The core updates frame length M0101, the host can read M0101 to see how many more messages are left.

4.4.2 STACK CONTENTS

The BC stack contains up to 64 groups of 4-word command descriptors. Each command descriptor is composed of the following words:

	Name	Bit	Description
0	Block Status Word. Updated by Core*	15	End Of Message – Set to '1' by the core when the message has been complete.
		14	Start Of Message - Set to '1' by the core when the message has been started. In most cases, this bit is '1' after end of message if there is a 1553 bus-coupling problem.
		13	'0' – This message has been processed on Bus A. '1' – This message has been processed on Bus B.
		12	'1' – Error was found in the message. Bits 10, 9, 8, 3, 2, 1, 0 indicate cause of error.
		11	Status Set. One of the status bits (excluding BCST bit) of the status return was '1'. BCST bit works in either mask mode or compare mode. In mask mode it works like other mask bits on the BCST bit. In compare mode, Status set occurs if BCST bit is different from bit 5 of BC control word.

		10	Format Error. The returned echo from the RT contained 1553 violations. See bits 3, 2, 1, 0 for a more accurate guess of the source of the problem.
		9	Response timeout. The RT responded too late or didn't respond at all.
		8	Loop back failed. The nature of 1553 bus is that every word transmitted, is also echoed back. The core verifies that the echo is correct and equal to the transmitted word. If not, this bit is set to '1'. Tip: The source of this type of error could be transceiver fault, or bus coupling problem.
		7	Unmasked Status bit set. This bit will be set to '1' if one of the status bits are set high and its appropriate mask bit in the BC control word is unmasked ('0'). BCST bit influences only in mask mode. See registers section for description of BCST bit.
		6	'1' indicates that two retries were performed.
		5	If bit 6 is '0' then a '1' indicates one retry was performed.
		4	Good data block received by BC. '1' – after an RT-BC, RT2RT, and Transmit Mode code with data commands if the message ended OK. '0' – after other message types, or if the above type of message was invalid. Loop back test failure does not cripple this bit result.
		3	'1' – The RT responded with wrong RT address.
		2	'1' – The RT transmitted a wrong number of words.
		1	'1' – Incorrect sync type response by RT.
		0	'1' – Invalid word. Indicates that the RT responded with a word containing 1553 errors.
1	Time Tag Word	15..0	16 bit real time counter incremented every 64 us. Written by core when the message started.
2	Gap to next message	15..0	Number of microseconds until start of next command. If gap shorter than message (0 for example), gap to next message would be the default as if this feature is off.
3	Message Pointer *	15..0	Points to the starting memory location of a message to be transmitted – the Message Block. The first word of the Message Block is the BC control word. The host sets this value. Core does not change it.

* The core has a built-in memory protection mechanism. If the Message Pointer (4th word) pointes to an address lower than 0x0108 than it is a wrong address. The message would not be processed, and the block status word would read 0xD000 that indicates the stack command was wrong.

The following diagram describes the order by which the stack information and pointers are updated during a message transfer. The time flows from left to right. Notice, SOM and EOM change, Stack Pointer update and T1 being updated.

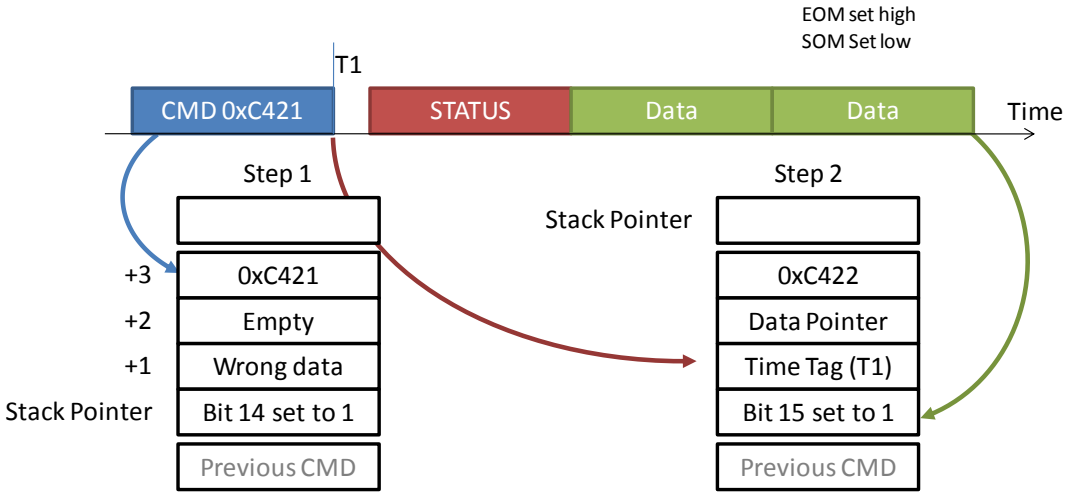

Figure 6: Stack Filling Up

The following diagram describes the usage of the inter-message gap feature provided by the 3rd word in the stack entry.

If the gap were shorter than the message length (0 for example), gap to next message would be the default (~10 us) as if this feature is off.

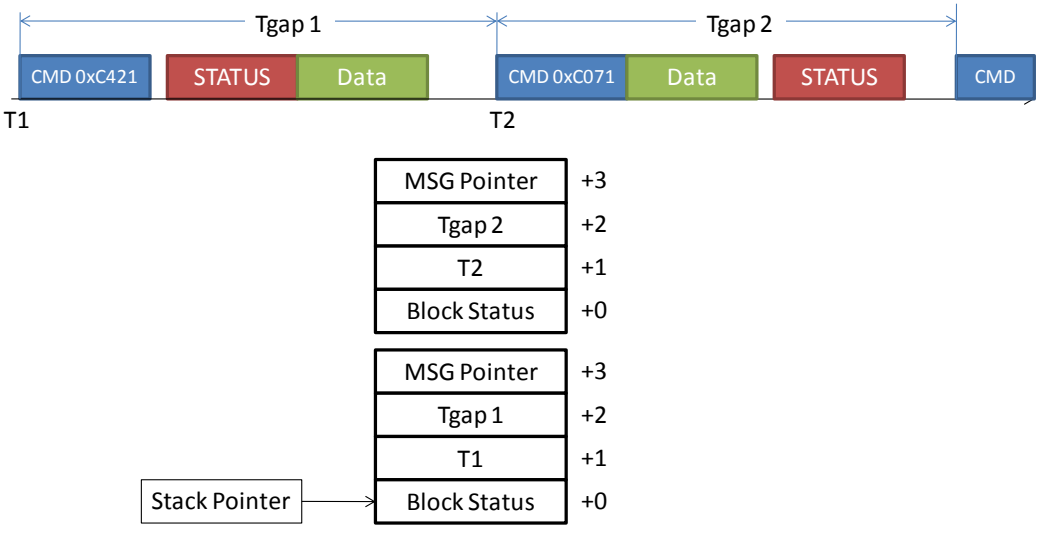

Figure 7: 3rd Word Gap Time

4.4.3 THE MESSAGE BLOCK

The Message Pointer points to the message block. The host should load the message block with the relevant words for the message.

The first word is not transmitted. The first word is the BC control word. This control word describes various modes of operation for the specific message as detailed ahead.

The structure of the message block varies according to the settings in the BC control word and the message type and length. The following table defines the message block contents types. Each entry is a 16bit word.

CONT – control word (not transmitted).
CMD – Command
STS – Status word
DAT – Data word
BCST - Broadcast
{DAT} – replication 1 to 32 Data words depending on word count.
XXX**LB** – Echo loop back of last transmitted word XXX

Color-coding:

Blue – loaded by Host before START command.
Green Italic – written by core after message transferred.

Type	Data Stack Contents
BC => RT	CONT CMD { DAT } *DATLB STS*
RT => BC	CONT CMD *CMDLB STS { DAT }*
RT => RT	CONT CMDrx CMDtx *CMDtxLB STStx { DAT } STSrx*
BC => Mode w/o data	CONT CMD *CMDLB STS*
BC => Mode transmit data	CONT CMD *CMDLB STS DAT*
BC => Mode receive data	CONT CMD DAT *DATLB STS*
BC => BCST	CONT CMD { DAT } *DATLB*
RT => BCST	CONT CMDrx CMDtx *CMDtxLB STStx { DAT }*
BC => BCST Mode w/o data	CONT CMD *CMDLB*
BC => BCST Mode data	CONT CMD DAT *DATLB*

The maximum length is 38 words. RT2RT command is composed of => 32 data + 2 commands + 2nd command loop-back + 2 status' + control word. For this reason the data area of the memory is divided into 38 word slices, but this is optional to be defined by the user.

4.4.4 THE BC CONTROL WORD

The first word in a message block is the BC control word. This word is not transmitted to the 1553 bus. This control word describes various modes of operation for the specific message as detailed.

Bit	Description
15	Transmit internal time tag in Synchronize with data mode command: '1' - Use time tag counter as data. '0' - Use data word in message block.
14	'1' – Mask Message Error (ME) bit in status word. '0' – No masking. If ME is set, this will cause "Status Bit Set" condition.
13	'1' – Mask Service Request (SR) bit in status word. '0' – No masking. If SR is set, this will cause "Status Bit Set" condition.
12	'1' – Mask busy bit in status word. '0' – No masking. If busy is set, this will cause "Status Bit Set" condition.
11	'1' – Mask Sub-System Flag (SSF) bit in status word. '0' – No masking. If SSF is set, this will cause "Status Bit Set" condition.
10	'1' – Mask Terminal Flag (TF) bit in status word. '0' – No masking. If TF is set, this will cause "Status Bit Set" condition.
9	'1' – Mask Reserve bits (RSRV) in status word. '0' – No masking. If RSRV is set, this will cause "Status Bit Set" condition.
8	'1' – Retry enable. Perform retry if message fails. The number of retries and the retry bus is defined in configuration registers 1 and 2.
7	'1' – Transmit on bus A. '0' – Transmit on bus B.
6	'1' – Perform internal loop back test. Message does not go out to 1553 bus but rather loop backed just like the normal echo of the transceiver. Of course the RTs do not reply. The host can check that the Loop back word has arrived correctly and that the loop back error flag is not set. Of course, other error bits should be masked because most likely they will be set.
5	If R08B11='1', i.e., Mask mode for BCST bit then this bit is the mask bit: '1' - will mask checking BCST bit '0' - will verify BCST is not '1', otherwise "Status Set" condition found. ELSE in compare mode: This bit should be equal to BCST bit, else "Status Set" condition found.
4	'1' – End OF Message Interrupt Enable (if not masked by interrupt mask register).
3	Ignored. Should be '0' for future compatibility.
2	'1' – The message is a mode command format (ignored by core)**.
1	'1' – The message is a BCST message format (ignored by core)**.
0	'1' – The message is an RT2RT command format.

** Core detects Mode command type and BCST command type from the command bits value regardless of the setting of these bits.

Note: RT2RT mode command format is supported. DDC devices do not support this mode. This is message type is typically not used.

5 MISCELLANEOUS

5.1 MECHANICAL DRAWINGS

72 Pins PQFP Package:

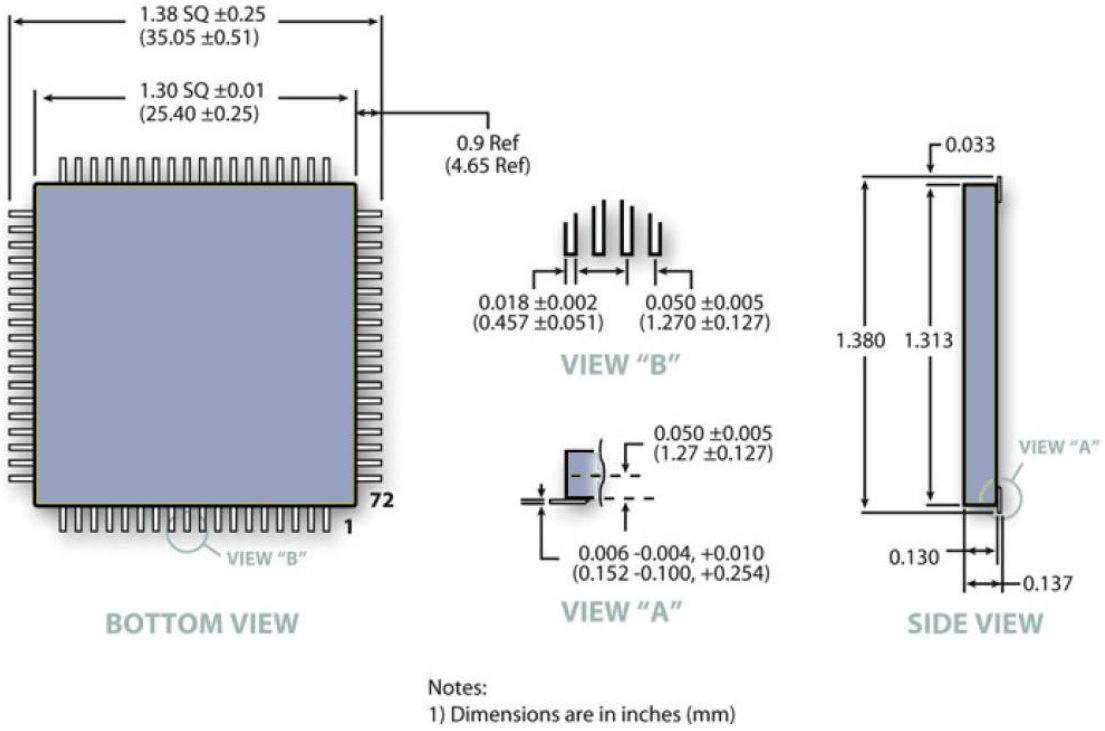

Figure 8: Mechanical Drawings

5.2 ORDERING INFORMATION

OCT-65178-G725-I

Part Number	Temperature Range
I	-40^{0}C to +85^{0}C
C	0^{0}C to 75^{0}C

Part Number	Packaging and Operating Voltage
G725	72 Pins PQFP Package, 5V VCC
G723	72 Pins PQFP Package, 3.3 VCC (Logic), 5V (Transceiver)

Part Number	Product Type	Clock Freq.	RAM (x 16 bits)
OCT-65178	RT Only	16/12 MHz	4K RAM
OCT-61588	BC/RT/MT	16/12 MHz	4K RAM
OCT-65179	RT/RT_BOOT	10/12/16/20 MHz	4K RAM
OCT-61688	BC/RT/MT	12/16 MHz	64K RAM
OCT-61689	BC/RT/MT	10/20 MHz	64K RAM

APPENDIX A: CHANGES TRACKING

First version of this manual: 6.22

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