

# 5 MHz MIL-STD-1553 IP Core, Transceiver and Transformer



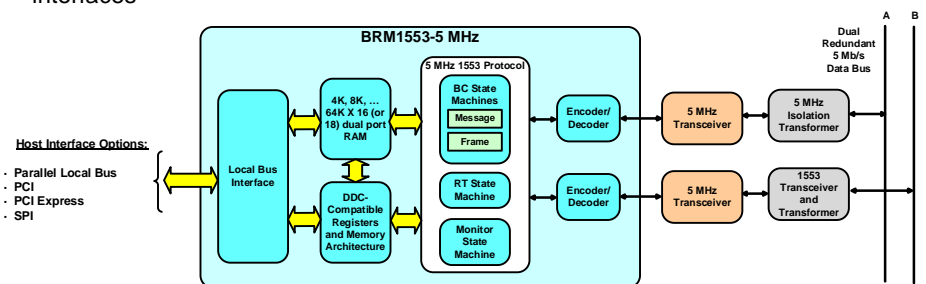
## BRM1553-5MHz

### 5 MHz MIL-STD-1553 IP Core, Transceiver and Transformer

### 5 Mb/s Data Rate with Standard MIL-STD-1553 Protocol operating over multi-drop bus topology

#### Key Features and Benefits

- 5 Mb/s Data Rate using standard MIL-STD-1553B protocol over “1553-like” multi-drop topology with 70 to 85 ohm twisted/shielded cable
- MIL-STD-1553 Intellectual Property Core for FPGAs and ASICs
- Supplied with transceivers and isolation transformers for 5 Mb/s operation
- Provides 1553 BC, RT, MT and RT/MT operating modes
- Architecturally compatible with DDC® Enhanced Mini-Ace® and Micro-Ace® and operates with Sital API/library/driver software
- Parallel Local Bus, 33/66MHz PCI, 1x PCI Express or SPI back-end interface
- Small FPGA area utilization
- Modular architecture allowing flexible implementations
- Provided as vendor and technology independent VHDL netlist code
- Configurations available: Simple Front-End, Local Bus, PC, PCIe and SPI interfaces



The BRM1553-5MHz IP core, transceiver and transformer are ideal for applications where it's desirable to leverage MIL-STD-1553's familiar multi-drop bus topology, protocol and hardware-level and API software interfaces, but requiring a higher data rate than 1 Mb/s. This IP core, transceiver and transformer operate over standard MIL-STD-1553 70 to 85 ohm twisted/shielded cable and provide a 5 Mb/s data rate.

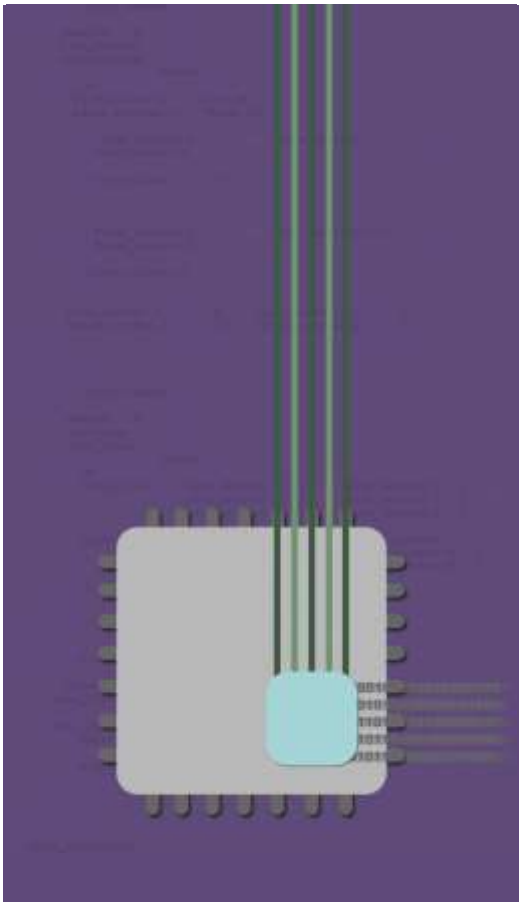
The BRM1553-5MHz IP core is based on Sital's popular BRM1553D MIL-STD-1553 core. This includes providing the same register and memory hardware/software interface as the BRM1553D and offers several host interface options. These include a local, parallel synchronous interface, PCI, PCI Express and SPI. If necessary, Sital can provide a “simple system” type interface with no memory and not requiring a host processor. In addition, Sital can also provide additional types of host interfaces and other features that customized and optimized in order to satisfy specific requirements.

For support of the BRM1553-5MHz IP core, Sital offers API/library/driver software. Sital's MIL-STD-1553 API consists of over 150 low-level and high-level function calls for use in BC, RT, Monitor or RT/Monitor modes. Sital can provide its API/library with drivers for VxWorks 6.9, 7.0 or 653; Linux 3.0, LynxOS, Pico/Linux or Petalinux; Windows; PikeOS, Green hills Integrity or bare metal (no OS). The software is provided with full documentation and sample programs.

More information available at [www.sitaltech.com](http://www.sitaltech.com)

#### More products from Sital:

- MIL-STD-1553 Components
- Mil-STD-1553 Boards
- MIL-STD-1553 Testers
- MIL-STD-1553 Design Services
- More IP Cores:
  - ARINC 429 IP Core
  - EBR 1553
  - H009, WB-194
  - CAN Bus



## Specifications

### Compatibility

- Protocol is in accordance with MIL-STD-1553B Notice 2, scaled for 5 MHz operation
- 5 Mb/s Data Rate
- Includes IP core, 5 Mb/s transceiver and isolation transformer, providing a trapezoidal waveform
- DDC® Enhanced Mini-ACE®/Micro-ACE®/Total-ACE® Register bits and Memory Architecture

### Host Interface Options

- High-performance synchronous, dual port RAM interface
- "DDC®" asynchronous interface
- 33MHz (66MHz optional), 32-bit PC target
- 1X PCI Express target
- SPI
- "Simple system" interface, with no memory, for systems with no processor

### RAM (BRM1553PCI & BRM1553D)

- 4, 8, 16, 32, 64K by 16 bits Dual Port RAM (Limited by FPGA resources only)
- Includes RAM parity generation and checking

### Clock

- Any even frequency from 12MHz and higher (12, 14, 16... 98, 100MHz, ...)
- Including 33MHz for PCI and 125MHz for PCI Express implementations

### Supported FPGAs

- Any FPGA with sufficient number of LUTs and dual-port memory
- FPGA families from the following vendors: Xilinx, Intel/Altera, Lattice, and Microsemi

\* For other FPGAs or ASICs, please consult Sital

### Deliverables

- FPGA manufacturer and family VHDL netlist format
- User's manual
- Sample VHDL code that incorporates the core
- Synthesis script for sample code
- Transceivers and transformers

### Part Numbers:

**Base Part Number:** BRM1553-5MHz For **DO-254 DAL A Certifiable Version:** BRM1553-5MHz

### Drivers for BRM1553-5MHz

- Windows XP – 32Bits
- Windows 7, 8, 8.1, 10 – 32 & 64Bits
- Linux – 32 & 64Bits:  
P/N: DRV1553LNX-32-64
- VxWorks 7.0:  
P/N: DRV1553VXW-7.0
- Others: LynxOS, Pico/Linux or Petalinux; Windows; PikeOS, Green hills Integrity or bare metal (no OS).

## 5 MHz MIL-STD-1553 IP Core, Transceiver and Transformer

### Manchester Decoder

The unique Manchester decoder can work with any clock, reduce the number of clock sources and clock domains on board (reduces EMI/RFI). This enables a high-performance synchronous interface between the host and the IP's shared memory.

Advanced algorithms for filtering out noise and disturbances enable the core to operate in harsh environments.

### BC Architecture

- Highly Autonomous BC, with Built-In Message Sequence Control
- Frame Scheduling
- Branching
- Asynchronous Message Insertion
- General Purpose Queue
- User-defined Interrupts

### RT Architecture

- Options for Single, Double and Circular Subaddress Buffering, and Global Circular Buffering
- Interrupt Status Queue
- 50% Circular Buffer Rollover Interrupts

### Monitor Architecture

- Selective Message Monitor
- Filtering based on Address, T/R Bit, and Subaddress
- Separate Command and Data Stacks
- 50% and 100% Stack Rollover Interrupts

### Transceiver and Transformer

- Based on Proven 1 Mb/s design, modified for 5 Mb/s
- 5 Mb/s Trapezoidal Transmitter Waveform aligns with MIL-STD-1553
- Transceiver and Isolation Transformer Meet 1553 Requirements for Waveform, Isolation and Common Mode Rejection

### Advanced Verification

To ensure a fully reliable and robust product the core was developed using an advanced verification environment that includes a Random-Generation engine, Code-Coverage and assertion tools.

All 1553 protocol, functions and performance requirements were verified.

### Third Party Validation

He 5 Mb/s version of Sital's MIL-STD-1553 IP core is based on the standard 1 Mb/s MIL-STD-1553 core that has successfully passed the full MIL-STD-1553B Notice 2 RT Validation test, based on the test plan from MIL-HDBK-1553A.

Validation tests were performed by an independent third-party laboratory.

If required, Sital can supply a DO-254 DAL A certified version of the BRM1553-5MHz IP core and DO-178 DAL A versions of its API/library/driver software.

### Simple Integration

In order to simplify the integration of the core, a sample VHDL design that uses the core is provided, including:

- Comprehensive user's manuals.
- A VHDL gate level model of the core for the target technology.
- A Transceiver VHDL model that connects the core with a dual redundant data bus.
- A bus tester VHDL model that generates 1553 messages and checks the return replies.
- Test bench that instantiates all of these components to a working example.
- A simulation script for compiling and running the core.

### About Sital

Sital Technology provides world-class products and expertise for communication bus applications in the avionics, aerospace and automotive industries. Sital embeds its vast experience and proficiency in its products which include MIL-STD-1553 and other avionics IP cores, components, boards and testers, as well as CAN bus devices and applications. With its highly-experienced staff of experts, the company's Projects Division undertakes design, integration and turn-key engagements on behalf of the world's leading commercial and military avionics companies, space agencies, and automobile designers and manufacturers. Sital's bus technologies and expertise improve robustness and efficiency as they lower cost, space and resource utilization.

Sital's formidable customer list includes leading military and commercial organizations throughout the world among them: NASA, Boeing, Lockheed-Martin, Honeywell, Raytheon, General Motors, British Aerospace, Thales, ECIL(India), Aselsan, Elbit, Rafael and IAI.

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