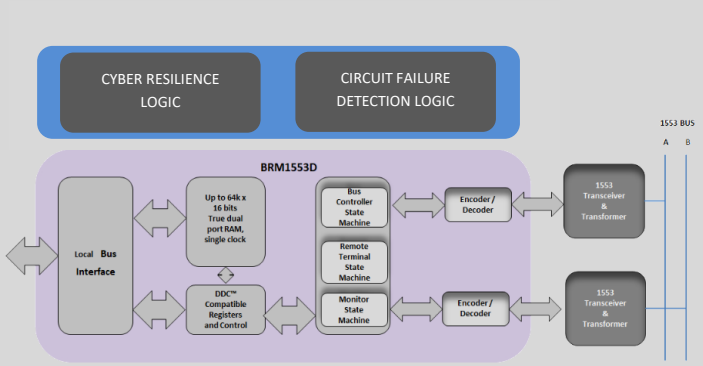
Safe and Secure MIL-STD-1553B/1760 IP Core

Product Overview:

The Safe and Secure BRM1553D-CS IP Core ("**BRM1553D-CS**") is an implementation of a MIL-STD-1553B/1760 compliant digital controller interface with built in cyber resilience and circuit failure detection capabilities. The BRM1553D-CS offers advanced network security and health monitoring capabilities while maintaining compliance with industry standards and peripherals devices (e.g –transceivers and magnetic transformers).



Key Features:

- MIL-STD-1553B/1760 compliant.
- Works with any COTS transceiver and transformer.
- CPU Interface (PCI/local bus/SPI)
- DDC compatible API interface for Enhanced MiniACE, MicroACE devices.
- Up to 16x64k internal memory.
- BC/RT/MT implementations.
- DO-254 DAL A certification ready artifacts

Applications:

- Avionics
- Munitions
- Weapons bus
- Space

Supported FPGA Families:

- Xilinx
- Lattice
- Altera/Intel
- Microsemi

Safe and Secure Enhanced Features:

- BC spoofing detection on bus A + bus B
- RT to BC message spoofing
- RT to RT message spoofing
- Message Source Validation (roadmap)
- Malicious/suspicious message invalidation (roadmap)
- Real-time Passive-TDR info to all connected matrixes and RIU/UUTReal-time.
- Circuit Fault Detection with TDR data

FREE EVALUATION

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Key Benefits:

- Real-time network security and monitoring
- Insightful forensic information for easy security playbook execution
- No software changes required
- Improve aircraft operational readiness time with insightful circuit failure root cause analysis.

Core Deliverables:

- FPGA agnostic VHDL Netlist for any clock frequency
- Simulation test bench
- HSID documentation
- API layer – ANSI C code
- Linux AXI bus driver
- Sample application – ANSI C code
- Vivado project files (Xilinx only)