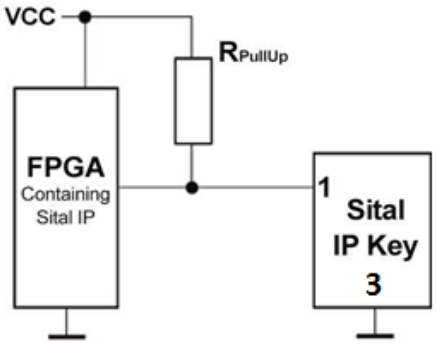
MIL-STD-1553B
BRM1553D HARDWARE KEY LICENSE

HARDWARE AUTHENTICATION KEY

Operating any of the Sital's IP Cores requires an authentication Hardware Key.
The Hardware Key uses a 3-pin SOT23 package (2.65mm x 2.9mm), One pin is connected to GND (Pin 3) and another pin (Pin 1) should be connected to the security pin at the FPGA, This pin should also be connected to a pull-up resistor (R_{PUP}), please refer to the 'Hardware Key Electrical Characteristics' table below for the appropriate value to be used per the specific design. Pin 2 remains not connected.
The authentication Hardware Key is part of the IP core and the user must assign a bi-directional pin at the FPGA to support this key.

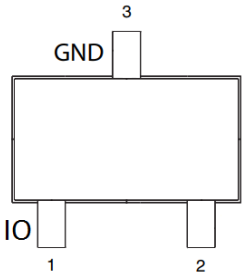
Operating Circuit



VCC supply in the range of 1.7V to 3.6V

Pin Configuration

Top View



Pinout:
Pin 1 ---------- IO
Pin 2 ---------- Not Connected
Pin 3 ---------- GND

Hardware Key Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pullup Voltage	V_{PUP}		1.7		3.6	V
Pullup Resistance	R_{PUP}	V_{PUP} = 1.7V	130		200	Ω
		V_{PUP} = 2.7V	0.2		1.8	kΩ
		V_{PUP} = 3.6V	0.33		4	kΩ
Input Capacitance	C_{BUS}				1000	pF
Input Load Current	I_L	V_{PUP}=3.6V		0.2	0.5	mA
Input Low Voltage	V_{IL}		-0.6		0.5	V
Input High Voltage	V_{IH}		V_{PUP} x0.7		V_{PUP} +0.5	V
Output Low Voltage	V_{OL}	I_L =4mA	0		0.4	V

Hardware Key Absolute Maximum Ratings

I/O Voltage to GND	-0.6V to V_{PUP} + 0.5V
DC Output Current	5mA
Operating Temperature Range	-40°C to +85°C
Temperature under Bias	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Hardware Key Synthesis Procedure

The IP core VHDL net list embeds a single PAD for the signal “to_key” that connects to the external key. If you are synthesizing your design with a synthesizer and you are making the 1553 IP core a black box, your synthesizer will not know that a PAD is inside the black box and will embed a buffer for that pin. You must then issue a NOPAD command for that pin in your VHDL code. For every synthesizer this is unique. Please refer to its manual for instructions.

In Precision Synthesis, use the NOPAD attribute.

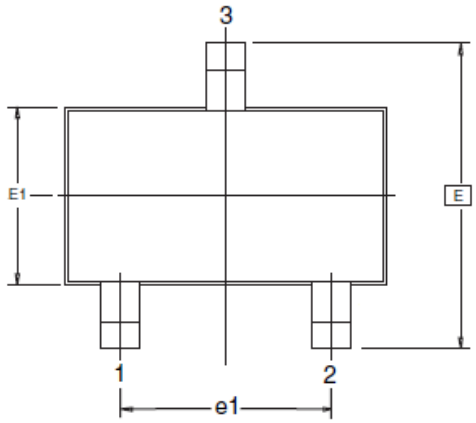
If your synthesizer reads your HDL code and the VHDL provided for the core, this operation is not required.

Hardware Key Ordering Information

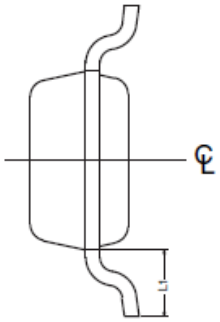
Keys will be provided in accordance with orders of the IP Core use licenses, See Ordering Information for details.

Hardware Key Mechanical Drawing

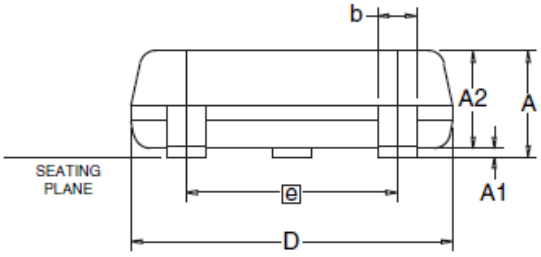
3-lead SOT23



Top View



End View



Side View

Top Marking	DESCRIPTION # Channels
K1-AU	1x1553
K1-BU	2x1553
K1-CU	3x1553
K1-DU	4x1553
K1-EU	5x1553
K1-FU	6x1553
K1-GU	7x1553
K1-HU	8x1553

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX
A	0.89	-	1.12
A1	0.01	-	0.10
A2	0.88	-	1.02
D	2.80	2.90	3.04
E	2.10	-	2.64
E1	1.20	1.30	1.40
L1	0.54 REF		
e1	1.90 BSC		
b	0.30	-	0.50

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
BRM1553D-HWLIC-XXX-YYY-Z	BRM1553D HW key type Z for company XXX for YYY Project

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