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ARINC 429 Transmitter & ARINC 429 Receiver IP Cores

User's manual

Ver 1.1

Sital Technology
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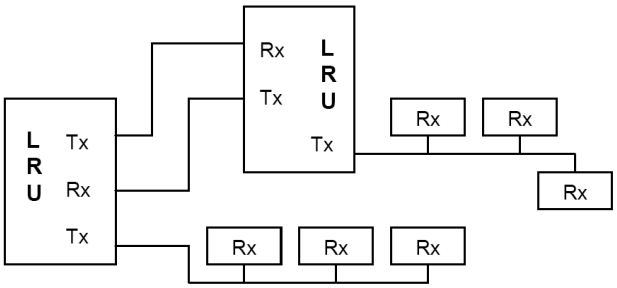
ARINC 429 Overview

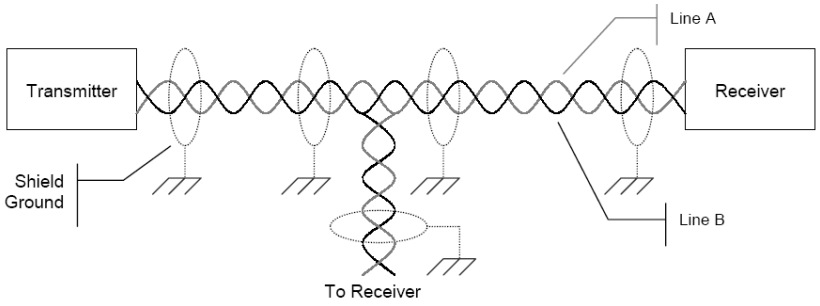
General Description

The ARINC 429 Specification defines the standard requirements for the transfer of digital data between avionics systems on commercial aircraft.
ARINC 429 hardware consists of a single transmitter connected to 1-20 receivers. Data can be transmitted in one direction only. Transmission from the transmitter is comprised of 32 bit words containing a 24 bit data portion (containing the actual information), and an 8 bit label (describing the data itself).
ARINC 429 employs unidirectional transmission of 32-bit words over two wire twisted pairs using bipolar RZ format. Messages are transmitted at a bit rate of either 12.5 or 100 kilobits per second to other system elements, which are monitoring the bus messages. Sequential words are separated by at least 4 bit times of null or zero voltage. By utilizing this null gap between words, a separate clock signal is unnecessary.



ARINC 429 Characteristics

The transmission bus media uses a 78 Ω shielded twisted pair cable. The shield must be grounded at each end and at all junctions along the bus.



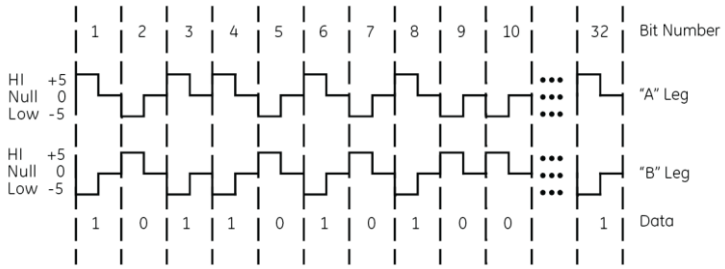
The transmitting source output impedance should be 75 Ω ± 5 Ω divided equally between Line A and Line B. This balanced output should closely match the impedance of the cable. The receiving sink must have an effective input impedance of 8k Ω minimum.
Maximum length is not specified, as it is dependent on the number of sink receivers, sink drain and source power. Most systems are designed for under 150 feet, but conditions permitting, can extend to 300 feet and beyond.

ARINC 429 specifies two speeds for data transmission. Low speed operation is stated at 12.5 kHz, with an actual allowable range of 12 to 14.5 kHz. High speed operation is 100 kHz ± 1% allowed. These two data rates cannot be used on the same transmission bus.
Data is transmitted in a bipolar, Return-to-Zero format. This is a tri-state modulation consisting of HIGH, NULL and LOW states. Transmission voltages are measured across the output terminals of the source.

Transmit & Receive voltage:

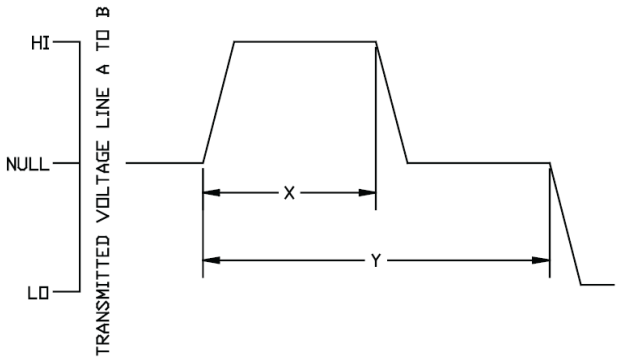
TRANSMIT	STATE	RECEIVE
+10.0 V ± 1.0 V	HIGH	+6.5 to 13 V
0 V ± 0.5V	NULL	+2.5 to -2.5 V
-10.0 V ± 1.0 V	LOW	- 6.5 to -13 V

Bit Encoding Example:



Bit Characteristics:

Parameter	High Speed	Low Speed
Bit Rate	100K bits/second	12.5K-14.5K bits/second
Time Y (one bit)	10 µsec ± 2.5%	1÷(bit rate) µsec ± 2.5%
Time X	5 µsec ± 5%	Y/2 µsec ± 5%
Pulse Rise Time	1.5 ± 0.5 µsec	10 ± 5 µsec
Pulse Fall Time	1.5 ± 0.5 µsec	10 ± 5 µsec



Slew Rates and Bit Timing Diagram

ARINC 429 Word Format

ARINC 429 is a very simple, point-to-point protocol. There can be only one transmitter on a wire pair. The transmitter is always transmitting either 32-bit data words or the NULL state. There is at least one receiver on a wire pair; there may be up to 20.
In most cases, an ARINC message consists of a single data word. The label field of the word defines the type of data that is contained in the rest of the word.
ARINC 429 data words are 32 bit words made up of five primary fields:
> Parity – 1 bit
> Sign/Status Matrix (SSM) – 2 bits
> Data – 19 bits
> Source/Destination Identifier (SDI) – 2 bits
> Label – 8 bits
ARINC convention numbers the bits from 1 (LSB) to 32 (MSB):

MSB																												LSB
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P	SSM		MSB									Data									LSB	SDI		Label							

The only two fields definitively required are the **Label** and the **Parity bit**, leaving up to 23 bits available for data representation.

Parity - The MSB is always the parity bit for ARINC 429. Parity is normally set to odd.

SSM - Bits 31 and 30 contain the Sign/Status Matrix or SSM.

Data - Bits 29 through 11 contain the data, which may be in a number of different formats.
In some cases, the data field overlaps down into the SDI bits. In this case, the SDI field is not used.

SDI - Bits 10 and 9 provide a Source/Destination Identifier.

Label - Bits 8 through 1 contain a label identifying the data type and the parameters associated with it. The label is used to determine the data type of the remainder of the word and, therefore, the method of data translation to use. Labels are typically represented as octal numbers.

When transmitting data words on the ARINC bus, the Label is transmitted first, MSB first, followed by the rest of the bit field, LSB first. Bit transmission order looks like this:

8, 7, 6, 5, 4, 3, 2, 1, 9, 10, 11, 12, 13 … 32.

8	7	6	5	4	3	2	1	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Label								SDI		LSB									Data									MSB	SSM		P

ARINC 429 Word Transfer Order

First transmitted bit

The Label is always transmitted first, in reverse order to rest of the ARINC word. The receiving Unit is responsible for data translation and regrouping of bits into proper order.

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ARINC 429 Transmitter IP Core

Features

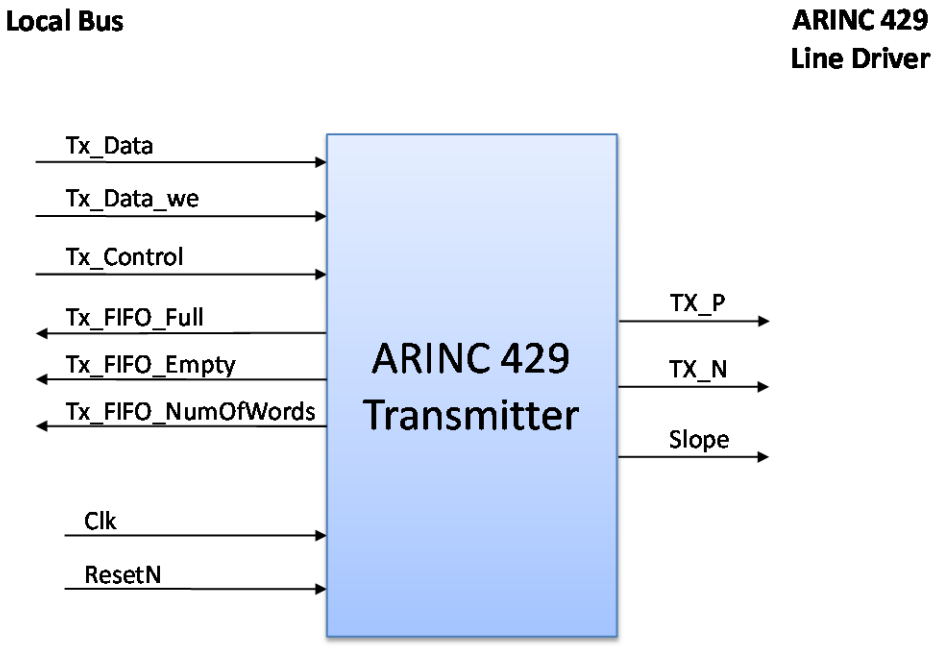
- ARINC 429 specification compatible.
- 32bits wide, programmable depth, FIFO buffer to hold xmitted data.
- Configured transmission baud rate.
- Programmable parity: Even, Odd or No-parity (32nd bit as data).
- FIFO full/empty indication.
- Supports Standard Line Drivers.

Operation

The ARINC_429_Tx_Core has a 32bits wide FIFO memory.
FIFO depth should be programmed during synthesis by setting the Tx_FIFO_Depth generic parameter. Default value is 64 words.

Whenever a data is written into to the Tx_FIFO, the ARINC_429_Tx_Core will start transmitting this data to the serial Tx ports based on the Tx channel control register configuration. Data will be transmitted consequentially word after word until the Tx_FIFO will become empty.
Tx_FIFO status (Empty/Full) and Number_Of_Words are reported in the dedicated ports.
Once FIFO_Full is asserted, there is no option to write new words to the Tx_FIFO.

Interface



Port Description

Signal Name	length	I/O	Description
To ARINC 429 Line Driver (such as HOLT HI8585)			
TX_P	1	Out	ARINC 429 TX Positive Serial data out to Line Driver Device. The TX_P signal is set to the logic 0 state upon a Reset operation and when there is no transmission.
TX_N	1	Out	ARINC 429 TX Negative Serial data out to Line Driver Device. The TX_N signal is set to the logic 0 state upon a Reset operation and when there is no transmission.
Slope	1	Out	Control the slope of the ARINC Line Driver differential output signal. '1' – Line driver rise and fall times are 1.5µs. '0' – Line driver rise and fall times are 10µs.
Local Bus			
Clock	1	In	Clock in. Any positive whole number > 2 Mhz.
ResetN	1	In	An active low signal that asynchronously resets all of the FFs in the core. Once the ResetN is deasserted, the ARINC_429_Tx_Core starts to operate.
Tx_Data	31 : 0	In	32 bits Data Bus, Parallel Data In to be loaded to the ARINC 429 Tx_FIFO.
Tx_Data_we	1	In	Data Write Enable, logic '1' for 1 clk cycle will write the Tx_Data from the local bus to the ARINC 429 Tx_FIFO.
Tx_control	7 : 0	In	8 bits configuration signal to control the ARINC_429_Tx_Core operation mode. (Parity kind, Transmission Baud Rate)
Tx_FIFO_Full	1	Out	'1' – ARINC 429 Tx_FIFO is full no more data can be written. '0' – ARINC 429 Tx_FIFO is not full.
Tx_FIFO_Empty	1	Out	'1' - ARINC 429 Tx_FIFO is empty. '0' – ARINC 429 Tx_FIFO is not empty.
Tx_FIFO_NumOfWords	Tx_FIFO_AD_bits-1:0	Out	Number of words currently in the Tx_FIFO.

Core Parameters

The ARINC_429_Tx_Core has the following top-level VHDL parameters (generics):

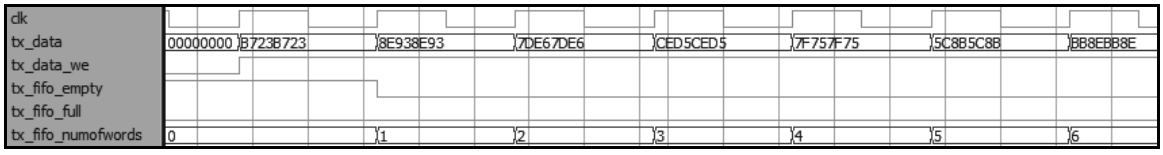
Parameter Name	Type	Description
Clk_freq	positive	A positive whole number (bigger than 1) designating the clock frequency in Mhz which is connected to the ARINC_429_Tx_Core.
Tx_FIFO_AD_bits	positive	Number of bits in the Tx_FIFO Address bus. Will set the depth of the Tx_FIFO based on the following formula: 2^ Tx_FIFO_AD_bits -1

Configuration

ARINC 429 Tx_Control bit configuration:

Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data rate 12.5 Khz								0
Data rate 100 Khz								1
No Parity (32nd bit as data)						X	0	
Even Parity						0	1	
Odd Parity						1	1	

Tx_FIFO Write Timing

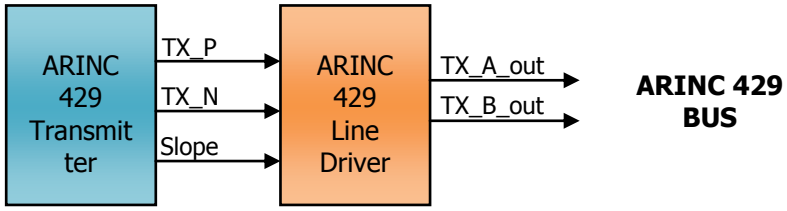


Tx_FIFO write cycles

TX Outputs

The ARINC_429_Tx_Core TX and Slope outputs should be connected to an ARINC 429 Line Driver such as HOLT HI-8585. The following table describes the ARINC_429_Tx_Core outputs (which are inputs to the Line Driver) and the Line Driver outputs respectively:

TX_P	TX_N	Slope	TX_A_out	TX_B_out	SLOPE
0	0	X	0V	0V	N/A
0	1	0	-5V	5V	10us
0	1	1	-5V	5V	1.5us
1	0	0	5V	-5V	10us
1	0	1	5V	-5V	1.5us
1	1	X	0V	0V	N/A



ARINC 429 Receiver IP Core

Features

- ARINC 429 specification compatible.
- Programmable labels recognition table (up to 256 labels).
- 32bits wide, programmable depth, FIFO buffer to hold received data.
- Support any whole number clock speed (multiplication of 1 Mhz)
- FIFO full/empty indication.
- Supports Standard Line Receivers.

Operation

The ARINC_429_Rx_Core has a 32bits wide FIFO memory.
FIFO depth should be programmed during synthesis by setting the Rx_FIFO_Depth generic parameter. Default value is 64 words.

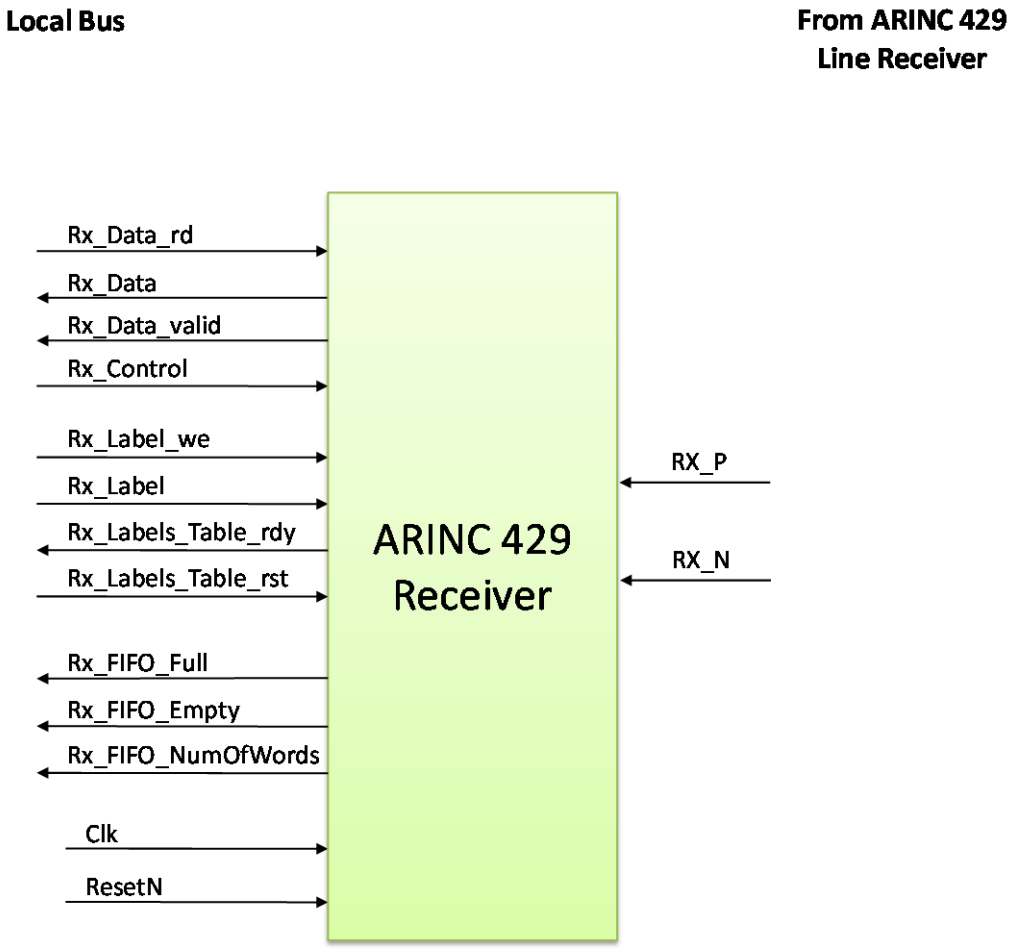
The ARINC_429_Rx_Core is programmed for the baud-rate of the input serial data and performs serial-to-parallel conversion and gap/parity check on the incoming data.
The received ARINC 32-bit word is checked for correct decoding and label matching (based on the label-compare bit and the SDI-compare bit in the Control Register) before loaded into the Rx_FIFO. ARINC words which do not meet the necessary matching ignored and are not loaded into the FIFO. The following table describes this operation:

label-compare CR(2)	ARINC word match label	SDI-compare CR(3)	ARINC word bits 9,10 match CR(7,8)	Rx_FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore data
1	No	1	Yes	Ignore data
1	No	1	No	Ignore data
1	Yes	1	Yes	Load FIFO

Rx_FIFO status (Empty/Full) and Number_Of_Words are reported in the dedicated ports.
Once Rx_FIFO_Full is asserted, new ARINC data words are ignored and not loaded to the Rx_FIFO.

A Labels Table stores up to 256 labels for label recognition. The ARINC_429_Rx_Core will compare the incoming label to the stored labels if label-compare is enabled. If a match is not found, the data is ignored with no indication. (Note that Label 00(Hex) is treated like any other label value, it has to be written to the Labels Table in order to be recognized).
The Rx_Label and Rx_Label_we signals are used to load labels into the Labels Table. Logic '1' for 1 clk cycle in the Rx_Label_we will load the Rx_Label value to the Labels Table.
Changing the Rx_Labels_Table_rst from 0 to 1 will initiate a reset Labels Table cycle.

Interface


Local Bus
From ARINC 429 Line Receiver
Rx_Data_rd
Rx_Data
Rx_Data_valid
Rx_Control
Rx_Label_we
Rx_Label
Rx_Labels_Table_rdy
Rx_Labels_Table_rst
Rx_FIFO_Full
Rx_FIFO_Empty
Rx_FIFO_NumOfWords
Clk
ResetN
ARINC 429 Receiver
RX_P
RX_N

Port Description

Signal Name	length	I/O	Description
From ARINC 429 Line Receiver (such as Holt HI8444)			
RX_P	1	In	ARINC 429 RX Positive Serial data in from Line Receiver Device.
RX_N	1	In	ARINC 429 RX Negative Serial data in from Line Receiver Device.
Local Bus			
Clock	1	In	Clock in. Any positive whole number > 2 Mhz.
ResetN	1	In	An active low signal that asynchronously resets all of the FFs in the core. Once the ResetN is deasserted, the ARINC_429_Rx_Core starts to operate and respond to the bus.
Rx_Data_rd	1	In	ARINC 429 Rx_Data read request, logic '1' for 1 clk cycle will follow with data from the Rx_FIFO (in case not empty).
Rx_Data	31 : 0	Out	32 bits Data Out Bus, Parallel Data from the Rx_FIFO. Data will be valid 1 clock after read request if FIFO is not empty.
Rx_Data_valid	1	Out	Data Valid will rise for 1 clock after Rx_Data_rd if FIFO is not empty.
Rx_control	7 : 0	In	8 bits configuration signal to control the ARINC_429_Rx_Core.
Rx_Label_we	1	In	Labe Write Enable, logic '1' for 1 clk cycle will load the Rx_Label value to the labels table.
Rx_Label	7 : 0	In	8 bits Data Bus, Parallel Label value to be loaded to the labels table.
Rx_Labels_Table_rdy	1	Out	'1' – Labels Table is rdy for write or Reset. '0' – Labels Table is busy.
Rx_Labels_Table_rst	1	In	Labels Table Reset. Rising detection on this input will reset the Labels Table.
Rx_FIFO_Full	1	Out	'1' – ARINC 429 Rx_FIFO is full, further ARINC data will be ignored. '0' – ARINC 429 Rx_FIFO is not full.
Rx_FIFO_Empty	1	Out	'1' - ARINC 429 Rx_FIFO is empty. '0' – ARINC 429 Rx_FIFO is not empty.
Rx_FIFO_NumOfWords	Rx_FIFO_AD_bits-1:0	Out	Number of words currently in ARINC 429 Rx_FIFO.

Core Parameters

The ARINC_429_Rx_Core has the following top-level VHDL parameters (generics):

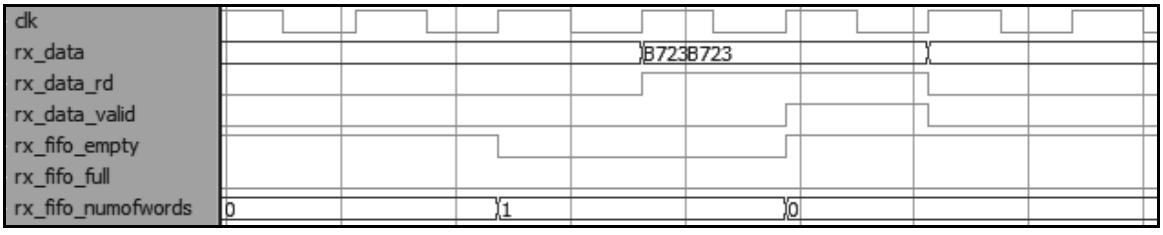
Parameter Name	Type	Description
Clk_freq	positive	A positive whole number (bigger than 1) designating the clock frequency in Mhz which is connected to the ARINC_429_Rx_Core.
Rx_FIFO_AD_bits	positive	Number of bits in the Rx_FIFO Address bus. Will set the depth of the Rx_FIFO based on the following formula: 2^ Rx_FIFO_AD_bits -1

Configuration

ARINC 429 Rx_Control bit configuration:

Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data rate 12.5 Khz								0
Data rate 100 Khz								1
No Parity (32nd bit as data)						X	0	
Even Parity						0	1	
Odd Parity						1	1	
Disable Label Recognition					0			
Enable Label Recognition					1			
Rx_Core Decoder Disabled				0				
Rx_Core Decoder Enabled (ARINC bit 9 must match Rx_Control bit 5 and ARINC bit 10 must match Rx_Control bit 6)				1				
If Decoder is enabled (Rx_Control Bit4=1) then ARINC bit 9 must match this bit			+					
If Decoder is enabled (Rx_Control Bit4=1) then ARINC bit 10 must match this bit		+						

Rx_FIFO Read Timing

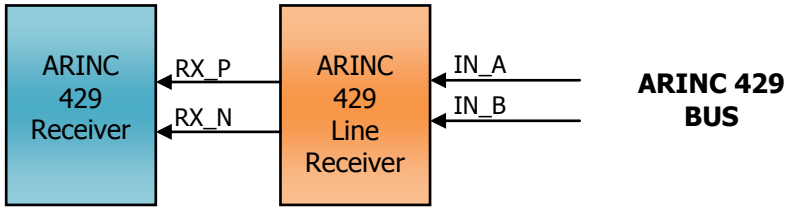


Rx_FIFO read cycle

RX Inputs

The ARINC_429_Rx_Core RX inputs should be connected to an ARINC 429 Line Receiver such as HOLT HI-8444. The following table describes the ARINC_429_Rx_Core inputs (which are outputs from the Line Receiver) and the Line Receiver inputs respectively:

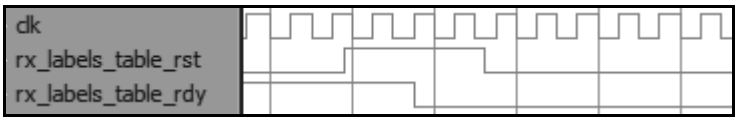
IN_A – IN_B	RX_P	RX_N
-2.5V to 2.5V	0	0
< -6.5V	0	1
> +6.5V	1	0



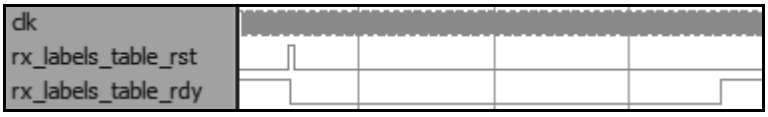
Labels Table Reset and Configuration Timing

The Rx_Label and Rx_Label_we signals are used to load labels into the Labels Table. The Rx_Labels_Table_rdy output signal should be high (logic '1') to enable label configuration or reset operation. This output goes low (logic '0') after Rx_Labels_Table_rst request till the end of the reset sequence.

Changing the Rx_Labels_Table_rst from 0 to 1 will initiate a Labels Table Reset cycle:

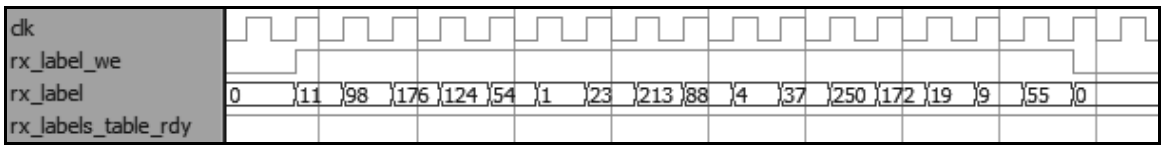


Rx_Labels_Table_rst request



Labels Table reset cycle

Logic '1' for 1 clk cycle in the Rx_Label_we signal will load the Rx_Label value to the Labels Table. (Rx_Labels_Table_rdy output signal should be high (logic '1') to enable this operation).



Rx Labels Table configuration cycle