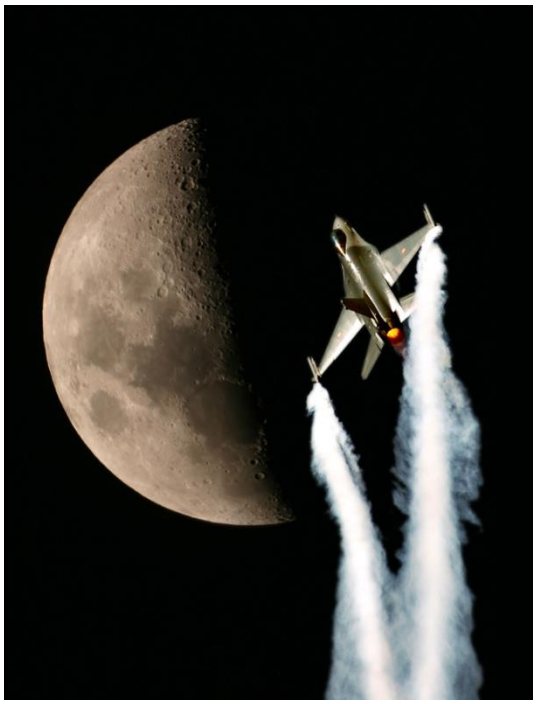
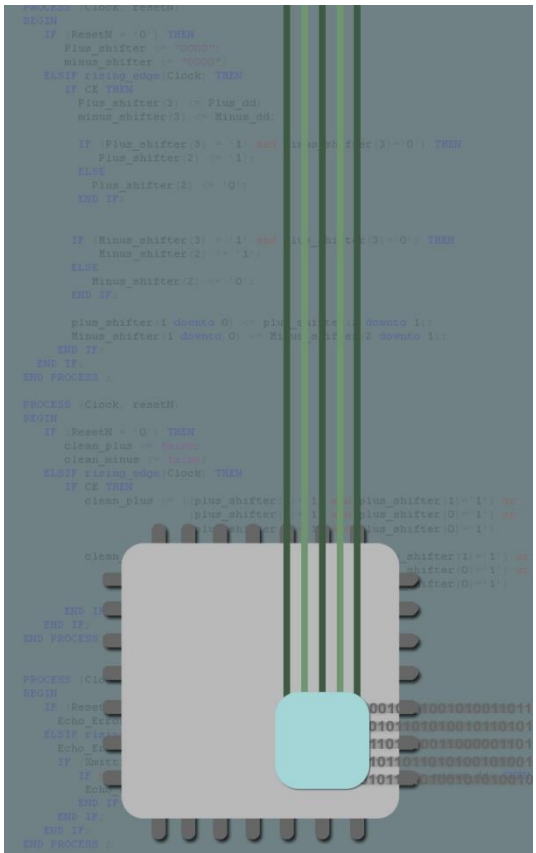
MIL-STD-1553 IP Core for FPGAs



BRM1553D

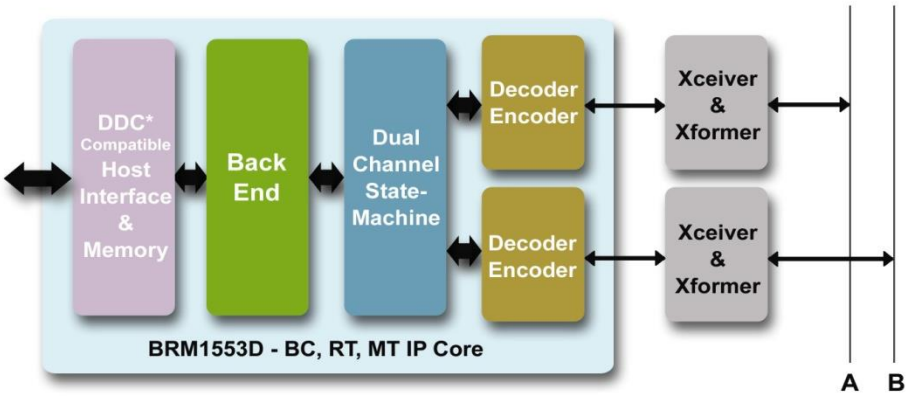
For 1553 Bus Controller, Remote Terminal and Monitor Terminal Implementations

Compact, Robust, Reliable
MIL-STD-IP-Cores



Key Features and Benefits

- Mil-Std-1553 Intellectual Property for FPGAs and ASIC
- Suitable for any MIL-STD-1553 BC, RT, MT implementation
- Compatible with *Enhanced DDC*® *Mini-Ace*® interface and functionality, works with existing software drivers
- Eliminates risks related to parts obsolescence
- Small FPGA area utilization
- Supports any even clock frequency
- Modular architecture allowing flexible implementations
- Provided with full verification environment
- Passed full RT validation testing by 3rd party
- Based on vendor and technology-independent VHDL code



Designed from the ground up for use in aerospace, avionics and military MIL-STD-1553 solutions, Sital's MIL-STD-1553 IP products, offer uniquely compact, robust and reliable BC, RT, MT solutions for any PLD/FPGA and ASIC device. They were developed based on the company's unflagging commitment to quality and excellence with strict adherence to meeting the stringent requirements of military and aerospace specifications.

More 1553 products from Sital

- *MIL-STD-1553 IP Cores for simple BC/RT Applications.*
- *MIL-STD-1553 Discrete Components Transceiver*
- *MIL-STD-1553 Obsolete Replacement Services*

More information available at **www.sitaltech.com**

SITAL Technology

BRM1553D

Specifications

Compatibility
- MIL-STD-1553B Notice 2
- RT Validated according to test plan from MIL-HDBK-1553A
- 1Mbps Data Rate
- Connects to any transceiver-transformer pair
- Enhanced DDC® MINI-ACE® interface

FPGA Requirements
- 10 pins to connect to transceiver
- Standard FPGA pads
- Internal FPGA Dual Port RAM of 2K x 16 or higher.

RAM
- 2, 4, 8, 16, 32, 64K by 16 bits
- Limited by FPGA resources only

Clock
- Any even frequency from 12MHz and up

Supported FPGAs
- Any FPGA with sufficient number of LUTs and memory
- FPGA families from the following vendors:
  - Xilinx
  - Actel
  - Altera
  - Lattice
  - QuickLogic

** For other FPGAs or ASIC please consult Sital*

BRM1553D Deliverables
- EDIF net list for the desired core (BC/RT/MT) for FPGA family and clock frequency
- User manual
- Sample VHDL code that incorporates the core
- Synthesis script for sample code

Available Configurations
- **BRM1553D-BCRTMT**: Bus Controller + Remote Terminal + Monitor Terminal
- **BRM1553D-RT**: Remote Terminal only
- **BRM1553D-RTMT:** Remote Terminal and Message/Word Monitor

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An FPGA Core for Any Mil-Std-1553 Implementation

The BRM1553D IP Core is suitable for any Mil-Std-1553 implementation. The core incorporates a backend logic that arranges the messages in a predefined memory structure, simplifying the interface between the 1553 bus and the local CPU. The BRM1553D core can act as a full replacement (2nd source) for DDC® enhanced mini-Ace® devices as the data is arranged in the same way.

Small Gate Count

Sital's BRM1553D requires very small space from FPGA for complex applications. The following table shows examples of the area usage, in different FPGA devices:

Vendor	Product Family	Area Usage (4-LUT count)	
		BC+RT+MT	RT Only
Altera	Stratix	4326	3257
	Cyclone	4330	3261
Xilinx	Virtex-II	4020	3066
	Spartan 3	4017	3063

- These numbers are approximate. Other FPGA vendors and families are available
- Actual area usage may vary according to core configuration.

Backend Interface

Includes *DDC's® Enhanced MINI-ACE®* interface, compatible with existing drivers and applications.
- No need to rewrite drivers code
- Eliminates replacement risk

Manchester Decoder

The unique Manchester decoder can work with any even clock frequency from 12Mhz and up to reduce clock sources and clock domains on board (reduces EMI/RFI).
Advanced algorithms for filtering out noise and disturbances enable the core to operate in harsh environments.

Advanced Verification

To ensure a fully reliable and robust product the core was developed using an advanced verification environment that includes a Random-Generation engine, Code-Coverage and assertion tools. All MIL-STD-1553B functions and performance requirements were verified.

3rd Party Validation

The BRM1553D IP Core successfully passed the full MIL-STD-1553B Notice 2 RT Validation test according to a test plan from MIL-HDBK-1553A.
Validation tests were performed by an independent 3rd party laboratory.

Simple Integration

In order to simplify the integration of the core, a sample VHDL design that uses the core is provided, including
- A comprehensive user manual
- A VHDL gate level model of the core for the target technology
- A Transceiver VHDL model that connects the core with 2 buses
- A bus tester VHDL model that generates 1553 messages and checks the return replies
- A top Test bench that instantiates all of these components to a working example
- A simulation script for compiling and running the core

About Sital Technology

Founded in 1993, Sital Technology is a leading provider of IP cores and products for Mil-Std-1553.

SITAL Technology's key quality resource is its creative, talented and professional staff. Our engineers are veterans of the Israeli Air Force, who served in the technical units of the F-16 avionics systems. They gained knowledge and experience with the MIL-STD-1553 standard from the bottom up, both as design engineers for MIL-STD-1553 components and as technicians working on the aircrafts.

Among our many customers you can find NASA, ESA, Thales, Orbital Science Corp., Elbit, Rafael, Israeli Aerospace Industries (IAI), Astronautics, Israeli Ministry of Defense, Elta, Honeywell, BAE Systems and many others.