SITAL TECHNOLOGY

BRM1553 FPGA IP Core Differences

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Selecting the right core for your MIL-STD-1553 application

Sital Technology offers several 1553 Remote Terminal (RT) and Bus Controller (BC) and Monitor (MT) FPGA IP cores ("**cores**"). These cores are intended for different applications. A proper selection of the right core would reduce design and maintenance efforts.

The BRM1553FE

BRM1553FE (Front-End) is an RT, BC or MT core intended for subsystems that need 1553 interface but the messages transferred to and from the RT are defined as "simple".

"Simple" means that every 1553 message is composed of a command pointing to a Sub Address (SA), and indicating the number of words for that SA. (i.e., SA is the paragraph, and the words are the sentences). If the words are dealt with individually for all the messages, then the RT is defined as simple.
On the other hand, if 2 or more words define a data record such that if one of the words of the record has errors then the whole record is an error, the messages could not be defined as simple.
For example: Assume an ICD (Interface Communication Document) for an F-16 camera RT uses two SAs. The first SA has one word. If this word's value is 0xAAAA, than the camera should start recording, and if its 0xBBBB it should stop. The second SA has two words for reading. The first word defines the Camera model. The second word indicates the tape position.
This application would be considered a simple RT and can use the BRM1553FE core saving the need for a CPU to control 1553 interface to the camera.
Usage of the BRM1553FE has shown dramatic development cost reductions gain by saving the need for a CPU and Software development, Hardware-software integration, and firmware maintenance.

An ICD that incorporates a SA with 3 words of which the first define a relative X position, the second word defines the Y position, and the third defines the Z position would not be considered a simple message. If, for some reason, only part of the message is transferred, the whole SA message should be dropped.
For these applications, the BRM1553D core should be used.

BRM1553D

The BRM1553D (DDC Enhanced MiniACE) is a superset of the BRM1553FE with a backend logic that arranges the messages in a predefined memory structure that will validate or invalidate a message on a message base rather than on a word base, as does the BRM1553FE.
The message managed of the BRM1553D is fully compatible with the approach used in the implementation of the DDC Enhanced MiniACE® design. This enables massive code reuse for implementers switching from DDC ASIC based designs to the BRM1553D FPGA based designs.

It should be noted that there are other / simpler ways to manage the message level control rather than the method used at the BRM1553D core, and these methods could be developed by the user logic that interfaces the BRM1553FE.

Sital can work with the user to suggest ways to implement different interfaces over the BRM1553FE core.

BRM1553PCI

The BRM1553PCI core is a superset of the BRM1553D. This IP core includes the DDC Enhanced MiniACE software interface, with PCI interface to the host CPU, saving the need for a PCI to local bus bridge.

BRM1553D-CS

The BRM1553D-CS core is a superset of the BRM1553D and is the world's first MIL-STD-1553B/1760 **Safe and Secure** IP core. This IP core includes the DDC Enhanced MiniACE software interface, with unique features to detect and prevent communication anomalies originating from wire faults or cyber attacks.

The BRM1553D-CS implements several unique passive technologies to provide real-time monitoring for anomalies at a logical level and even prevention capabilities for denial of service, unit spoofing, data manipulation and impersonation attacks.

In addition the BRM1553D-CS also has built-in and patented passive-TDR© technology to monitor real-time circuit failures on 1553 networks such as shorts and disconnects.

The IP core streamlines the information on anomalies with meaningful forensic data to optimize the threat analysis time and resources needed and for the rapid implementation of cyber resilience playbooks.

DO254BRM1553D

The DO254BRM1553D core is a special set of the BRM1553D which have passed DO254 DAL A certification. This IP core includes the DDC Enhanced MiniACE software interface.
The DO254BRM1553D has been verified by 3rd parties and qualified for DO-254 DAL A with a trusted third party LogiCircuit to supply the DO-254 artifacts under license. Customer may opt in to license the IP and independently work with a DER to create an internal certification artifacts package.

Comparison Table

	BRM1553FE / ERL	BRM1553D / BRM1553D-CS/ DO254BRM1553D	BRM1553PCI
Main Application	Simple 1553 interface (FE) Space, Radiation Tolerant (ERL)	Complex 1553 applications, DDC MiniACE, Enhanced MiniACE and uACE replacement .	Complex 1553 applications, DDC MiniACE, Enhanced MiniACE and uACE replacement, with PCI interface.
Compatibility	Mil-Std-1553B Notice 2	Mil-Std-1553B Notice 2 DDC Enhanced MiniACE Back-End	Mil-Std-1553B Notice 2 DDC Enhanced MiniACE Back-End 33/66MHz PCI bus interface
Available Modes	Bus Controller (BC) Remote Terminal (RT) Bus Monitor (MT) And any combination.	Bus Controller (BC) Remote Terminal (RT) Bus Monitor (MT) And any combination.	Bus Controller (BC) Remote Terminal (RT) Bus Monitor (MT) And any combination.
FPGA Requirements			
Area Utilization	764 to 1059 4-LUT, Depending on FPGA type	RT only: 2800 to 3400 4-LUT Depending on FPGA type BC + RT + MT: 3950 to 4320 4-LUT Depending on FPGA type	RT only: 3100 to 3700 4-LUT Depending on FPGA type BC + RT + MT: 4250 to 4620 4-LUT Depending on FPGA type
External Pins	10 pins to connect to transceiver Standard FPGA pins	10 pins to connect to transceiver Standard FPGA pins	10 pins to connect to transceiver Standard FPGA pins PCI bus interface (depending on configuration)
Memory Required	32 x 16 bits	2, 4, 8, 16, 32 or 64K x 16 bits	2, 4, 8, 16, 32 or 64K x 16 bits
Clock Frequency	Any even frequency of 12Mhz or more.	Any even frequency of 12Mhz or more.	33 or 66MHz
CPU Required	No	Yes	Yes
Device Drivers	No needed	VxWorks 7.0 VxWorks 653 Linux ThreadX PikeOS Integrity OS	VxWorks 7.0 VxWorks 653 Linux ThreadX PikeOS Integrity OS
Development Kits	BRD1553SPI (**SPI**) or Grip 2.0 USB with transceiver and transformers VHDL Evaluation Netlist	BRD1553SPI (**SPI**) or Grip 2.0 USB with transceiver and transformers VHDL Evaluation Netlist	BRD1553SPI (**SPI**) or Grip 2.0 USB with transceiver and transformers VHDL Evaluation Netlist