MINUET™ - Mil-Std-1553 Bus Controller, Remote Terminal & Bus Monitor Component

MNT1553PCI-8, MNT1553LB-8,
MNT1553PCI-16, MNT1553LB-16

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Revision History

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Rev 0.21	30/11/2010	Updated Pinout Tables, software interface	Duli	18

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Approved By:		

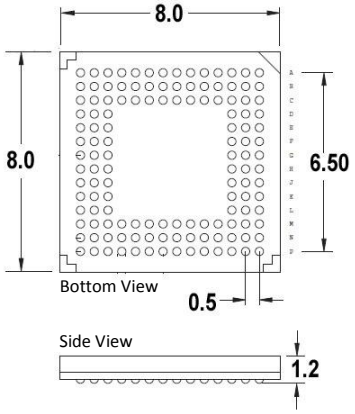
Contents

FEATURES

- **MIL-STD-1553B Notice 2 Compliant Terminals.**
  - Supports Bus Controller mode or simultaneous Remote Terminal/Monitor mode.
- **Software Compatible to DDC MiniACE®, Enhanced MiniACE® and µACE® Components.**
  - Software drivers used with any DDC® component can be used seamlessly with Minuet.
  - Provided also with software drivers and API, compatible to DDC® at the API level.
- **Smallest Solution Available - 8x8mm or 17x17mm BGA.**
  - 132-Ball csBGA (8x8 mm) or 256-Ball ftBGA (17 x17 mm) Package.
- **PCI or Local Bus Interface.**
  - 33/66MHz PCI bus interface, suitable for connecting directly to PCI bus.
  - Supports PCI burst mode.
  - Simple address/data bus for connecting to local CPU.
- **3.3V and 1.2V operation, very low power consumption.**
- **Operates from wide range of clock frequencies.**
  - 10, 12, 16, 20, 24, 32 and 40MHz available. 33/66MHz for PCI interface.
  - Customer may order specific clock frequency.
- **Flexible pinout configuration for easy PCB Layout.**
  - Customer may order different pinout configurations.
- **Very fast access 8K x 16 or 16K x 16 bits Shared RAM.**
  - True dual-port RAM for fast access to the device from CPU or PCI bus.
  - The 8mm package comes with 8K words of shared RAM and the 17mm package comes with 16K words of shared RAM.
  - Access to RAM can be synchronized to PCI or local bus clock, enabling burst read/write.
- **Bootable RT option required for MIL-STD-1760.**
  - Supports 'Busy' bit at status word during CPU boot.
  - RT Address is set by discrete bits.
- **PCI Evaluation board available – BRD1553PCI.**
- **Provided with Luthier™ - software tool for 1553 bus operation.**

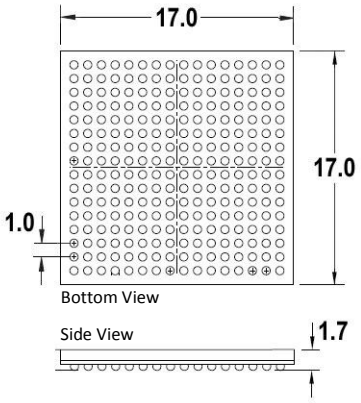
PRODUCT SELECTION OPTIONS

- **MNT1553PCI-8 / MNT1553LB-8**



  - 8mm X 8mm, 132-Ball csBGA package
  - 0.5mm pitch
  - 8K Words of internal memory
  - PCI or local bus interface

- **MNT1553PCI-16 / MNT1553LB-16**



  - 17mm X 17mm 256-Ball ftBGA package
  - 1mm pitch
  - 16K Words of internal memory
  - PCI or local bus interface

INTRODUCTION

General Description

"Minuet" is family of 8mm sqr or 17mm sqr Mil-Std-1553 protocol terminals, which include Bus Controller, Remote Terminal and Monitor, compatible with DDC MiniACE, Enhanced MiniACE and uACE interfaces.

A Minuet device is able to work in conjunction with any standard 1553 transceiver, or with Sital's discrete transceiver. For example, when working with NHI's Bus+, a complete 1553 solution includes an 8mm component and 2 Bus+ transceiver/transformer components, making this the smallest available solution for 1553.

Minuet is available in several configurations:

- 8mm sqr, BC/RT/MT, 8K Words of internal RAM and local bus interface.
- 8mm sqr, BC/RT/MT, 8K Words of internal RAM and PCI interface.
- 17mm sqr, BC/RT/MT, 16K Words of internal RAM and local bus interface.
- 17mm sqr, BC/RT/MT, 16K Words of internal RAM and PCI interface.

Minuet offers several benefits over existing Mil-Std-1553 components, including very small size, flexible interface, low power consumption, flexible clock frequency and compatibility to existing software drivers and applications.

The approach offered by Sital, to separate the 1553 protocol interface from the 1553 analog front-end, enable users for better flexibility when designing their system or layout their PCB. For example – the Minuet component can be physically close to the PCI connector, while the 1553 transceiver and transformer can be near the 1553 connector. The signals in between Minuet and 1553 transceiver are less sensitive to Signal Integrity issues than PCI signals or 1553 signals.

Sital provides several tools for better use of Minuet, including the Minuet evaluation board (BRD1553PCI) and the Luthier™ software tool for managing 1553 communications bus via Minuet devices.

All Minuet components work at industrial temperature range of -40C to +85C.

Back-End Interface

The Minuet family offers two separate ways of back-end interface – PCI and Local Bus.

The Local Bus interface contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus.

The PCI interface is a standard PCI Target interface compliant with PCI 2.2 standard.

The memory management scheme for RT mode provides three data structures for buffering incoming and outgoing data. Combined with the Minuet's extensive interrupt capability, these structures serve to ensure data consistency while off-loading the host processor. The Minuet devices can optionally boot-up as a RT with the Busy bit set for 1760 applications. The Minuet BC mode implements several features aimed at providing an efficient real-time software interface to the host processor including automatic retries, programmable inter-message gap times or message rate, automatic frame repetition, and flexible interrupt generation.

Interface to the 1553 Bus

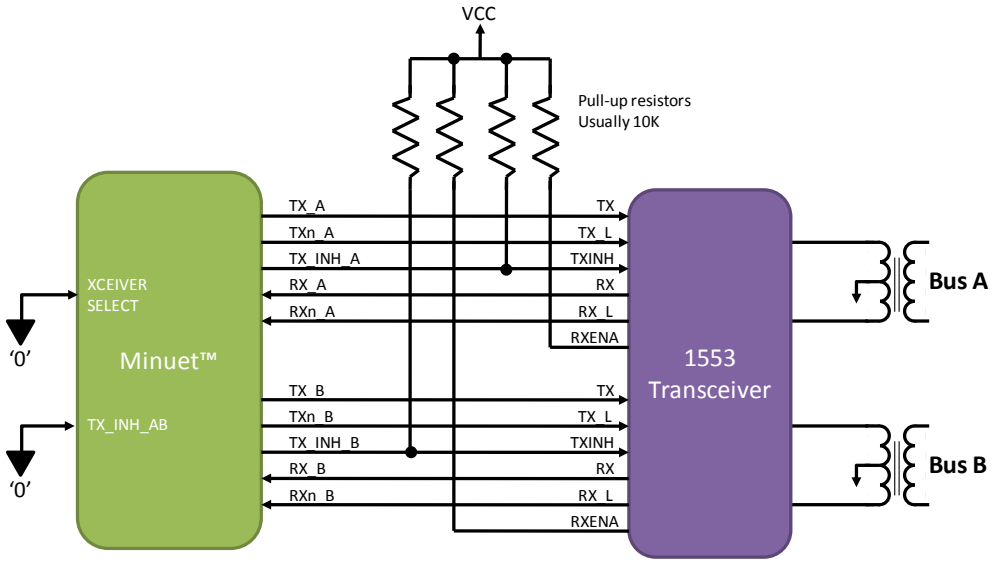
The Minuet™ components require external 1553 Transceiver and a coupling transformer.

Minuet™ can work with any existing 1553 transceiver, or with Sital's Discrete components transceiver design.

For example, together with National Hybrid's (NHI) BUS+, Transceiver and Transformer packed together, this is the smallest available total solution for 1553 bus. Any Holt or NHi 7mm dual transceiver or DDC single transceiver can also be used for space saving purposes.

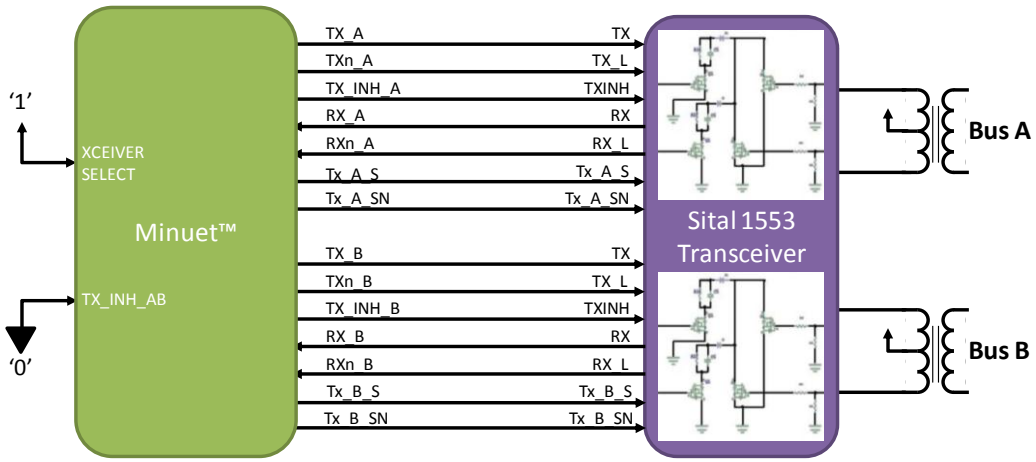
A "Transceiver_Select" pin is used to select between a standard transceiver and Sital's Discrete transceiver.

In case a standard transceiver is used, then each channel should be connected directly from/to Minuet in the following manner:



Note that VCC and logic levels must be compatible. Because Minuet uses 3.3V interface, then it is best to use a 3.3V transceiver as well.

When used with Sital Discrete Components Transceiver, then the channels should be connected as follows:



Software Interface

General Description

The interface to the device is divided between several control registers and memory access. The registers are used to control the device and its operation, while the memory is used as the 1553 message interface and control.

The registers are mapped to address 0x0 to 0x20 and can be written or read (depending on their functionality). Memory can be 8K or 16K (depending on model) – all by 16 bits.

Access to the registers or memory is done through the same address and data lines. When on PCI mode, then memory and registers are mapped to a different base address. When Local-Bus mode, when accessing the registers, the MEM/REG signal should be kept low, and when accessing the memory this signal should be high.

There are several dependencies between the configuration of registers and the configuration and operation of the memory. The user must verify that all dependencies configured correctly with accordance to the required operation of the device.

Registers Operation

The software interface of Minuet to the host processor consists of 20 internal operational registers for normal operation. These registers determine the device configuration, modes of operation, memory structure, interrupt control and status, etc.

The address mapping for the registers is detailed in the following table:

PCI Address	Local Bus Address Lines					Register Description (Read/Write)
Base +	A4	A3	A2	A1	A0	
0x 00	0	0	0	0	0	Interrupt Mask Register #1 (RD/WR)
0x 01	0	0	0	0	1	Configuration Register #1 (RD/WR)
0x 02	0	0	0	1	0	Configuration Register #2 (RD/WR)
0x 03	0	0	0	1	1	Start/Reset Register (WR)
0x 03	0	0	0	1	1	RT Command Stack Pointer (RD)
0x 04	0	0	1	0	0	RT Subaddress Control Word Register (RD)
0x 05	0	0	1	0	1	Time Tag Register (RD/WR)
0x 06	0	0	1	1	0	Interrupt Status Register #1(RD)
0x 07	0	0	1	1	1	Configuration Register #3 (RD/WR)
0x 08	0	1	0	0	0	Configuration Register #4 (RD/WR)
0x 09	0	1	0	0	1	Configuration Register #5 (RD/WR)
0x 0A	0	1	0	1	0	(RD) – all '0'
0x 0B	0	1	0	1	1	Not relevant for RT – see BC mode manual for details
0x 0C	0	1	1	0	0	Not relevant for RT – see BC mode manual for details
0x 0D	0	1	1	0	1	RT Last Command (RD)
0x 0E	0	1	1	1	0	RT Status Word Register (RD)
0x 0F	0	1	1	1	1	RT BIT Word Register (RD)
0x 10	1	0	0	0	0	Not implemented
0x 11	1	0	0	0	1	Not implemented
0x 12	1	0	0	1	0	Not implemented
0x 13	1	0	0	1	1	Not implemented

0x 14	1	0	1	0	0	Not implemented
0x 15	1	0	1	0	1	Not implemented
0x 16	1	0	1	1	0	Not implemented
0x 17	1	0	1	1	1	Not implemented
0x 18	1	1	0	0	0	Configuration Register #6 (RD/WR)
0x 19	1	1	0	0	1	(RD) – all '0'
0x 1A	1	1	0	1	0	Front End version of Core (RD)
0x 1B	1	1	0	1	1	Back End version of Core (RD)
0x 1B	1	1	0	1	1	Not relevant for RT – see BC mode manual for details
0x 1C	1	1	1	0	0	BIT Test Status Register (RD)
0x 1D	1	1	1	0	1	Interrupt Mask Register #2 (RD/WR)
0x 1E	1	1	1	1	0	Interrupt Status Register #2 (RD)
0x 1F	1	1	1	1	1	Not relevant for RT – see BC mode manual for details

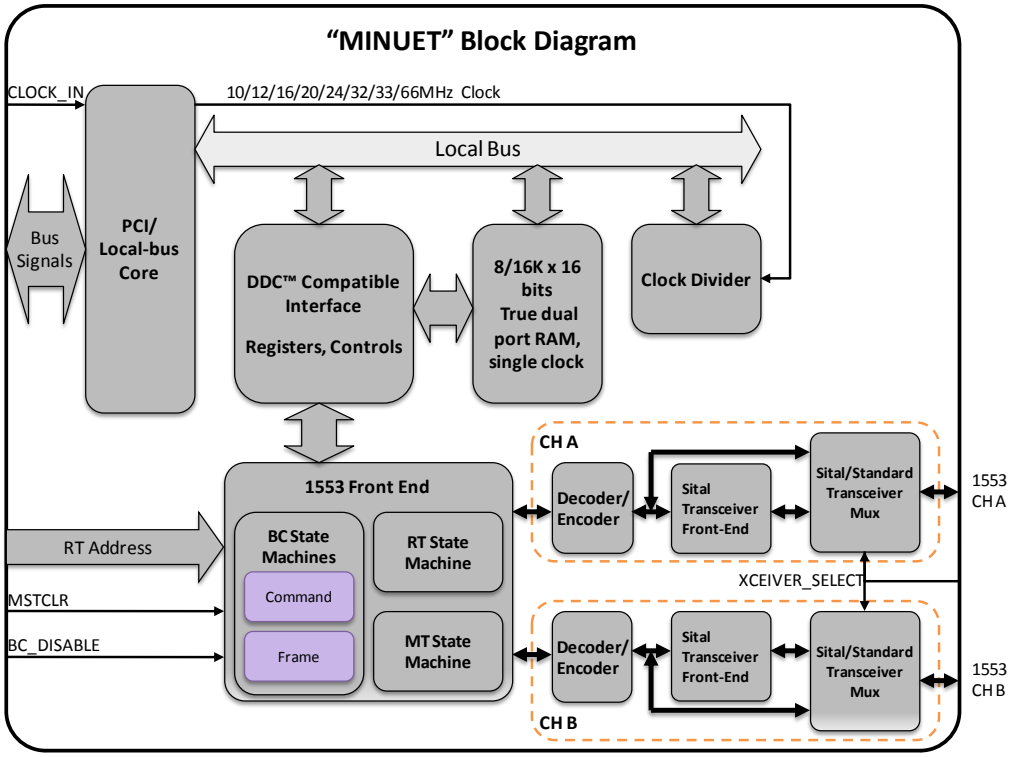
Note:
Not all of the bits of the DDC MiniACE registers are implemented. Please see "1553 Core compatibility" document for details on all differences between the 1553 Core and DDC MiniACE and Enhanced MiniACE.

Memory Data Structure and Modes of Operation

The data reception and transmission is controlled on a message-by-message basis. Each message is stored in the memory or read from the memory based on mapping defined by the CPU during offline state. The CPU sets up the mapping and modes of operations in the dual port RAM and in the configuration registers. The mapping options are discussed in the software manual.

ARCHITECTURE OVERVIEW

Figure 1: Minuet Block Diagram:



1553 Front-End: Each Minuet device contains a 1553 Front-End core which performs all the functionality of managing the Mil-Std-1553 protocol interface. This core is built of several state machines that follow the Mil-Std-1553B standard. There are separated state machines for Remote Terminal, Monitor and Bus Controller.

The RT state machine: The RT state machine identifies a set of bus words as a valid message, being 'transmit', 'receive', 'mode' or 'broadcast' message. When the RT State Machine decides it has to either store a word to the subsystem or fetch a word from the subsystem it interfaces through the DDC™ Compatible Interface to the Dual-Port RAM array, and stores or reads that word.

The Monitor state machine: The Monitor state machine searches for valid commands. When a command is found, the state machine checks whether this command defines a message required for monitoring. In such case, the state machine manages the process of storing the words one by one in the Dual-Port memory into a pre-defined location.

BC State Machine: When transmission is initiated the frame state machine manages the sequencing of a whole frame of messages as defined by the configuration registers and fixed memory locations in the memory. The frame is composed of a set of individual messages being transmitted and managed over the 1553 bus one after the other. The host also points the beginning of the first message in memory and defines how many messages to transact through 2 fixed location memory words. When all data has been loaded, and the state machines are idle, the host sends a START command. As a response, the frame state machine starts the frame transmission. The frame state machine fetches the messages from memory and forwards the requested message information to the command state machine which in turn sequences the command data and status words for a complete legal 1553 message. When the message is complete the frame state machine accesses the next command, and so on until all messages have been completed.

The command state machine either transmits words through the encoders or receives RT responses through the decoders. The encoders and decoders interface between the core's 16 bits parallel internal buses and the MuxBus serial bus.

Decoder/Encoders: The Front-End core is connected to two separate Decoder/Encoders, one for each dual-redundant 1553 channel, which translate the serial bus messages from the MIL-STD-1553 Manchester coding and format, into a 16 bit parallel data accompanied by status indications for each word. These Decoder/Encoders are carefully designed to overcome noise and other problems related to the 1553 bus.

Sital Transceiver Front-End: Minuet can be connected to any off-the-shelf transceiver or to Sital's discrete transceiver. The Sital transceiver requires some additional control logic, which is managed by the Sital Transceiver Front-End cores. These cores perform signal shaping, filtering and short-circuit protection for the Sital analog Front-End.

Users can select between the Sital discrete transceiver and the standard transceiver via the XCEIVER_SELECT pin, which controls the multiplexer between the Sital Transceiver Front-End core and the standard interface directly from the Decoder/Encoder.

DDC™ Compatible Interface block: The operation of the 1553 Front-End state machines is controlled by the DDC™ Compatible Interface block. This block contains the control registers and memory interface to the dual-port RAM. This block creates the control signals for the 1553 Front-End core. The registers and interface are explained in details in Minuet User's Manual.

Dual-Port RAM: The True Dual-Port RAM stores messages received or to be transmitted to the 1553 bus. The messages are arranged in memory with accordance to the DDC™ MiniACE memory structure.

The memory is a true dual port RAM, with both sides independently reading or writing data. When operating as Local Bus, the Host CPU should supply the memory control signals, address, data, chip select and write enable, synchronized with the clock signal supplied to the core. This synchronized approach will ensure robustness of operation. Since Minuet and the Host CPU work with the same clock, the design will have no transient effects. When operating as PCI interface, Minuet uses the PCI clock of 33MHz or 66MHz.

PCI/Local Bus Interface: Selection between PCI or local bus interface is depending on Minuet model. When PCI interface, the PCI IP core bridges between a 32 bit, 33Mhz or 66Mhz PCI bus and internal local bus.

PINS DESCRIPTION

PCI Mode (47 pins) – MNT1553PCI-8 and MNT1553PCI-16

Signal Name	In/Out	Description
AD[31:0]:	I/O	Address and Data are multiplexed onto these pins. AD[31:0] transfers a 32-bit physical address during "address phases", and transfers 32-bits of data information during "data phases".
C/BE[3:0]#:	I/O	Bus Command and Byte Enables are multiplexed onto these pins.
PAR	I/O	Parity is even parity over the AD[31:0] and C/BE[3:0]# signals.
FRAME#	I/O	Cycle Frame is driven low by the initiator to signal the start of a new bus transaction.
TRDY#	I/O	Target Ready is driven low by the target as an indication it is ready to complete the current data phase of the transaction.
IRDY#	I/O	Initiator Ready is driven low by the initiator as an indication it is ready to complete the current data phase of the transaction.
STOP#	I/O	Stop is driven low by the target to request the initiator terminate the current transaction.
DEVSEL#	I/O	Device Select is driven active low by a PCI target when it detects its address on the PCI bus.
IDSEL	In	Initialization Device Select is used as a chip select during PCI configuration read and write transactions.
CLK	In	Clock provides the timing reference for all transfers on the PCI bus. 33/66MHz.
RST#	In	Reset is driven active low to cause a hardware reset of a PCI device
M66EN	In	Selects between 33MHz and 66MHz bus clock.
INTA#	Out	Interrupts are driven low by the device to request attention from their device driver.

Local Bus Mode (37 pins) – MNT1553LB-8 and MNT1553LB-16

Signal Name	In/Out	Description
DATA[15:0]	I/O	16 Bits DATA bus I/O.
ADDRESS[13:0]	In	14 Bits Address bus input.
MEM/REG	In	Selects between memory access and register access.
MSTCLR	In	Master Reset for Minuet. Does not reset the memory content.
CLOCK_IN	In	Clock input. Clock Range is selected by M66EN pin: • Range 1: (M66EN='0') 10, 12, 16, 20MHz or • Range 2: (M66EN='1') 24, 32 or 40MHz
READYD	Out	When non-zero wait-state mode, logic '0' on this signal indicates to the host CPU that the read or write cycle is done.
IOEN	Out	I/O Enable – This signal is low when Minuet is performing the requested host bus cycle. Normally this signal should not be used.
SELECT	In	Active low chip select for the Minuet device for memory and register access.
RD/WR	In	During Read or Write cycle to the device, when this line is logic '1' then this is a read cycle. If this line is logic '0' then data from the data bus is written to the device.
M66EN	In	Select CLOCK_IN Range, Doubles the clock frequency. For example – when clock register is set to 16MHz, then the device will work with 32MHz clock. '0' – Clock Range 1; '1' – Clock Range 2.

1553 Pins (all Minuet components)

Signal Name	In/Out	Description
SSFLAG/EXT_TRIG	In	RT mode – When low sets the subsystem flag bit in the status word response. BC mode – A rising edge on this signal triggers a frame if external trigger enabled in configuration register #1.
BC_DISABLE	In	Disables the BC operation.
RTAD0-RTAD4	In	RT address. These pins determine the address of the RT on the 1553 bus.
RT_AD_P	In	RT Address Parity.
RT_AD_LAT	In	RT Address Latch. RT axddress is latched on rising edge.
RT_BOOT_n	In	When '0' Starts RT Mode in Busy Status.
XCEIVER_SELECT	In	Select between Sital and Standard transceiver.
Standard Transceiver		
TX_INH_AB	In	Transmitter inhibit input for the Channel A and Channel B MIL-STD-1553 transmitters. For normal operation, this input should be connected to logic "0". To force a shutdown of Channel A and Channel B, a value of logic "1" should be applied to the TX_INH input.
TX/TXn-A	Out	Positive and negative polarity of 1553 output signals for Bus A. These signals should be connected to a Mil-Std-1553 transceiver.
RX/RXn-A	In	In phase and negative received signals from transceiver, Bus A.
TX_INH_A	Out	Transmission inhibit signal connected to transceiver. This signal is normally high, and is asserted low by the core during transmission or if endless transmission error occurs.
TX/TXn-B	Out	Positive and negative polarity of 1553 output signals for Bus B. These signals should be connected to a Mil-Std-1553 transceiver.
RX/RXn-B	In	In phase and negative received signals from transceiver, Bus B
TX_INH_B	Out	Transmission inhibit signal connected to transceiver. This signal is normally high, and is asserted low by the core during transmission or if endless transmission error occurs.
Sital Transceiver (in addition to the above pins)		
Tx_A_SN, **Tx_A_S,** **Tx_B_SN,** **Tx_B_S,**	Out	Connects to Sital Technology transceiver signals. Should be left unused if COTS transceiver is used

MINUET PINOUT

PCI Mode – MNT1553PCI-8 and MNT1553PCI-16[1]

	MNT1553PCI-8	MNT1553PCI-16
Signal Name	Pin	Pin
AD31	A13	
AD30	A12	
AD29	A11	
AD28	B10	
AD27	A10	
AD26	B9	
AD25	A9	
AD24	B6	
AD23	A7	
AD22	C5	
AD21	A6	
AD20	C7	
AD19	A5	
AD18	C8	
AD17	A3	
AD16	C9	
AD15	M5	
AD14	P5	
AD13	M4	
AD12	P6	
AD11	N2	
AD10	P7	
AD9	N3	
AD8	P9	
AD7	P10	
AD6	N7	
AD5	P12	
AD4	N8	
AD3	P13	
AD2	N9	
AD1	P14	
AD0	N12	
C/BE3#	A8	
C/BE2#	A2	
C/BE1#	P4	
C/BE0#	N4	
$\overline{\text{STOP}}$	M7	
$\overline{\text{IRDY}}$	A1	
$\overline{\text{TRDY}}$	M10	
PAR	M6	
$\overline{\text{FRAME}}$	C10	
$\overline{\text{DEVSEL}}$	P2	
IDSEL	B3	

	MNT1553PCI-8	MNT1553PCI-16
Signal Name	Pin	Pin
$\overline{\text{INTA}}$	D13	
PCI_CLK	H14	
$\overline{\text{RESET}}$	B13	
M66EN	G3	
PCI/$\overline{\text{LB}}$	Not Applicable	
$\overline{\text{SSFLAG}}$/EXT_TRIG	D1	
BC_DISABLE	H3	
RTAD4	E1	
RTAD3	F1	
RTAD2	G1	
RTAD1	H1	
RTAD0	L1	
RT_AD_P	B2	
RT_AD_LAT	B1	
RT_BOOT	N1	
XCEIVER_SELECT	P1	
TX_INH_AB	F3	
TX-A	A14	
TXn-A	B14	
RX-A	D14	
RXn-A	E14	
TX_INH_A	F12	
TX-B	N14	
TXn-B	L14	
RX-B	G14	
RXn-B	F14	
TX_INH_B	G12	
Tx_A_SN	E12	
Tx_A_S	D12	
Tx_B_SN	H12	
Tx_B_S	J12	
VCCIO 3.3V	A4, A12, B5, B7, C3, C11, C14, F2, F13, J2, J14, K1, K12, M1, M3, M8, M9, M12, N5, N13, P1, P11	
Vcc 1.2V	B11, C4, J3, J13, N11, P8	
GND	B4, B8, C1, C6, C12, C13, E2, E13, J1, M2, M11, M14, N6, N10, P3	

1. MNT1553PCI-16 pinout not determined yet.

Local Bus Mode – MNT1553LB-8 and MNT1553LB-16[1]

	MNT1553LB-8	MNT1553LB-16
Signal Name	Pin	Pin
Data15		P6
Data14		T7
Data13		P7
Data12		T8
Data11		P8
Data10		T9
Data9		R6
Data8		T10
Data7		T11
Data6		R8
Data5		T12
Data4		R9
Data3		T13
Data2		R10
Data1		T14
Data0		R11
MEM/$\overline{\text{REG}}$		A12
Addr13		A6
Addr12		A11
Addr11		A5
Addr10		A10
Addr9		A4
Addr8		A9
Addr7		A2
Addr6		B6
Addr5		B1
Addr4		B4
Addr3		B2
Addr2		C4
Addr1		B3
Addr0		D4
$\overline{\text{READYD}}$		T5
$\overline{\text{IOEN}}$		N5
$\overline{\text{INT}}$		C1
$\overline{\text{SELECT}}$		B8
RD/$\overline{\text{WR}}$		R7
CLOCK_IN		B8
$\overline{\text{MSTCLR}}$		A13
M66EN		P10
PCI/$\overline{\text{LB}}$		D1

	MNT1553LB-8	MNT1553LB-16
Signal Name	Pin	Pin
$\overline{\text{SSFLAG}}$/EXT_TRIG		F1
BC_DISABLE		G1
RTAD4		L1
RTAD3		M1
RTAD2		N1
RTAD1		P1
RTAD0		R1
RT_AD_P		K1
RT_AD_LAT		J1
RT_BOOT		H1
XCEIVER_SELECT		A14
TX_INH_AB		E1
TX-A		G16
TXn-A		H16
RX-A		F16
RXn-A		E16
TX_INH_A		D16
TX-B		P16
TXn-B		R16
RX-B		N16
RXn-B		M16
TX_INH_B		L16
Tx_A_SN		C16
Tx_A_S		B16
Tx_B_SN		J16
Tx_B_S		K16
VCCIO 3.3V		C5, C12, E3, E7, E10, E14, G5, G8, G12, H10, J7, K5, K7, K9, K12, L7, M3, M7, M10, M14, P5, P12
Vcc 1.2V		G7, G9, H7, J10, K8, K10
GND		A1, A16, B5, B12, C8, E2, E15, H8, H9, H14, J3, J8, J9, M2, M15, P9, R5, R12, T1, T16

1. MNT1553LB-8 pinout not determined yet.

DC AND SWITCHING CHARACTERISTICS

Absolute Maximum Ratings [1, 2]

Supply Voltage V_{CC} . . . . . -0.5 to 1.32V
Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V
Input or I/O Tristate Voltage Applied[3] . . . . . -0.5 to 3.75V
Storage Temperature (Ambient) . . . . . -65 to 150°C
Operating Temperature . . . . . -40°C to +85°C
Junction Temperature Under Bias (Tj) . . . . . +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. All voltages referenced to GND.
3. Overshoot and undershoot of -2V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCIO}	I/O Driver Supply Voltage	3.135	3.465	V
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C

DC Electrical Characteristics

Over Recommended Operating Conditions:

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Logic '1' Output Voltage		V_{CCIO} -0.4	-	-	V
V_{OL}	Logic '0' Output Voltage		-	-	0.4	V
V_{IH}	Logic '1' Input Voltage		2.0	-	3.6	V
V_{IL}	Logic '0' Input Voltage		-0.3	-	0.8	V
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{CCIO}$	-	-	10	µA
		$V_{CCIO} \le V_{IN} \le V_{IH}$ (MAX)	-	-	150	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	-	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{CCIO}$	30	-	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	-	-	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	-30	-	-	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	-	-	210	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	-	-	-150	µA
V_{BHT}	Bus Hold Trip Points		V_{IL} (MAX)	-	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	-	8	-	pf
C2	Dedicated Input Capacitance	V_{CCIO} = 3.3V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	-	6	-	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active.
2. T_A 25°C, f = 1.0 MHz.

Supply Current at 25°C

Over Recommended Operating Conditions:

Symbol	Parameter	Device	Typical	Units
I_{CC}	Core Supply Current (1.2V)	MNT1553PCI-8	50	mA
		MNT1553LB-8	50	mA
		MNT1553PCI-16	60	mA
		MNT1553LB-16	60	mA
I_{CCIO}	I/O Driver Supply Current (3.3V)	MNT1553PCI-8	140	mA
		MNT1553LB-8	140	mA
		MNT1553PCI-16	150	mA
		MNT1553LB-16	150	mA

PART NUMBER DESCRIPTION

MNT1553PCI-8

Part Number	Memory Configuration
8	8K x 16 bits
16	16K x 16 bits

Part Number	Interface Selection
PCI	33/66MHz PCI Interface
LB	16 bits Local Bus

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