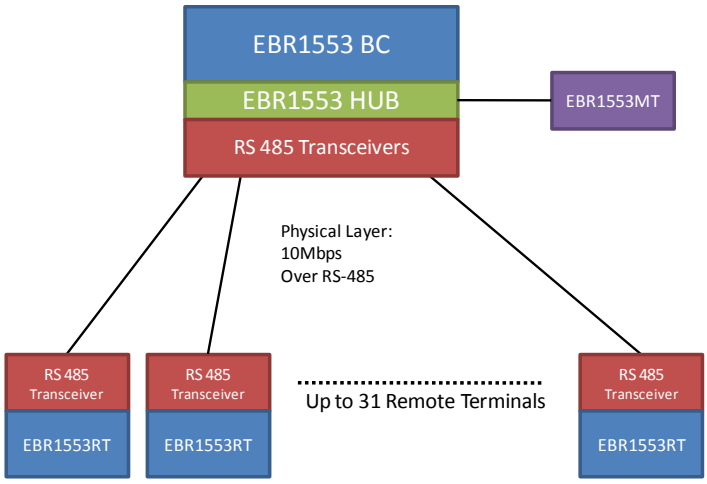
ENHANCED BIT RATE 1553 IP CORE FOR FPGA

FEATURES

- **10 Megabits per Second 1553 protocol Intellectual Property for FPGAs and ASIC**
- **Suitable for any EBR1553 BC, RT, MT implementation**
- **Back-end compatible to *DDC® Mini-Ace®* and *Enhanced Mini-Ace®* interface and functionality, works with existing software drivers**
- **Small FPGA area utilization**
- **Supports any even clock frequency**
- **Modular architecture allowing flexible implementations**
- **Provided with full verification environment**
- **Based on vendor and technology independent VHDL code**



APPLICATIONS

- **EBR1553 Remote Terminal.**
- **EBR1553 Bus Monitor.**
- **EBR1553 Bus Controller.**

DESCRIPTION

The EBR1553D IP Core is suitable for any Enhanced Bit Rate 1553 implementation. It incorporates decoder/encoder suitable for EBR1553 implementation over RS-485 physical interface.
The words received and transmitted are arranged in a dual port memory according to the memory mapping of the DDC® Enhanced mini-ACE®. The CPU controls the EBR1553D by programming the dual port memory for message specific settings, and programming a set of configuration registers for device wide controls.

The memory is a true dual port RAM as defined by the FPGA target, with both sides independently reading or writing data. The CPU should supply the memory control signals, address, data, chip select and write enable synchronized with the clock signal supplied to the core. This synchronized approach will ensure robustness of operation. Since the core and the user logic work with the same clock, the design will have no transient effects.

EBR1553D can be used on any FPGA, using any clock frequency and memory size. This ensures quick and reliable integration with user's design. The parametrically settable clock frequency can be set from 60 Mhz and up – reduces number of clock domains in design.

Designed from ground up for use in aerospace, avionics and military MIL-STD-1553 solutions, Sital's MIL-STD-1553 and EBR1553 IP products, offer uniquely compact, robust and reliable BC, RT, MT solutions for any PLD/FPGA and ASIC device. They were developed following the company's unflagging commitment to quality and excellence along with strict adherence to meeting the stringent requirements of the military and aerospace specifications.

* DDC® and MINI-ACE® are registered trademarks of Data Device Corporation, Bohemia, NY, USA. There is not any affiliation between Data Device Corporation and Sital technology, Ltd.

SUPPORTED FPGAS

The EBR1553D IP core can be used in most FPGA with sufficient number of LUTs and memory.
Currently the supported FPGA families are from the following vendors:

- Xilinx
- Actel
- Altera
- Lattice
- QuickLogic

** For other FPGAs or ASIC please consult Sital*

This parameter is set once by Sital during the synthesis for the customer and cannot be changed by the customer during operation. See Ordering Information for details.

BRM1553D DELIVERABLES

- An EDIF Netlist of the core for the target FPGA technology, clock frequency and memory size.
- A comprehensive user's manual.
- A top Test bench that instantiates all of these components to a working example, including:
  - A Transceiver VHDL model that connects the core with 2 buses.
  - A bus tester VHDL model that generates 1553 messages and checks the return replies.
- A simulation script for compiling and running the core.

17 Atir Yeda St., Kfar-Saba, ISRAEL 44643
Email: info@sitaltech.com
Website: http://www.sitaltech.com