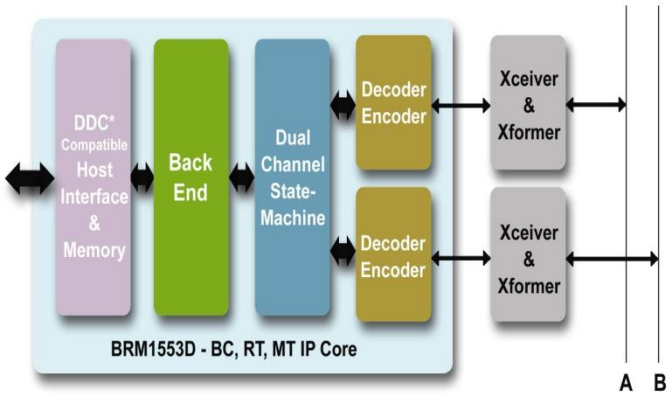
MIL-STD-1553B IP CORE FOR FPGA

FEATURES

- **Mil-Std-1553 Intellectual Property for FPGAs and ASICs**
- **Suitable for any Mil-Std-1553 BC, RT, MT implementation**
- **Compatible with *DDC*® *Mini-Ace*® and *Enhanced Mini-Ace*® interfaces and functionality, works with existing software drivers**
- **Eliminates risk related to part obsolescence**
- **Small FPGA area utilization**
- **Supports any even-clock frequency**
- **Modular architecture allowing flexible implementations**
- **Provided with full verification environment**
- **Passed full RT validation testing by 3rd party**
- **Based on vendor and technology-independent VHDL code**



APPLICATIONS

- **Mil-Std-1553 Remote Terminal**
- **Mil-Std-1553 Remote Terminal with Message Monitor**
- **Mil-Std-1553 Bus Controller**

DESCRIPTION

The BRM1553D IP Core is suitable for any Mil-Std-1553 implementation. The core incorporates a backend logic that arranges the messages in a predefined memory structure simplifying the interface between the 1553 bus and the local CPU. The BRM1553D core can act as a full replacement (2nd source) for DDC® ACE®, Mini-Ace® and Enhanced Mini-Ace® devices as the data is arranged in the same way*.

BRM1553D can be used on any FPGA, using any clock frequency and memory size. This ensures quick and reliable integration with user's design. The parametrically-settable clock frequency can be set from 12 Mhz and up – reduces number of clock domains in design.

The IP core is provided as an EDIF Netlist for the selected FPGA, Clock Frequency and memory configuration. It can be provided in any functional configuration, such as RT only, RT+MT, MT only or RT+MT+BC, saving space on FPGA and reducing none-required functionality.

Designed from ground up for use in aerospace, avionics and military MIL-STD-1553 solutions, Sital's MIL-STD-1553 IP products offer uniquely compact, robust and reliable BC, RT, MT solutions for any PLD/FPGA and ASIC device. They have been developed following the company's unflagging commitment to quality and excellence and with strict adherence to the stringent requirements of military and aerospace specifications.

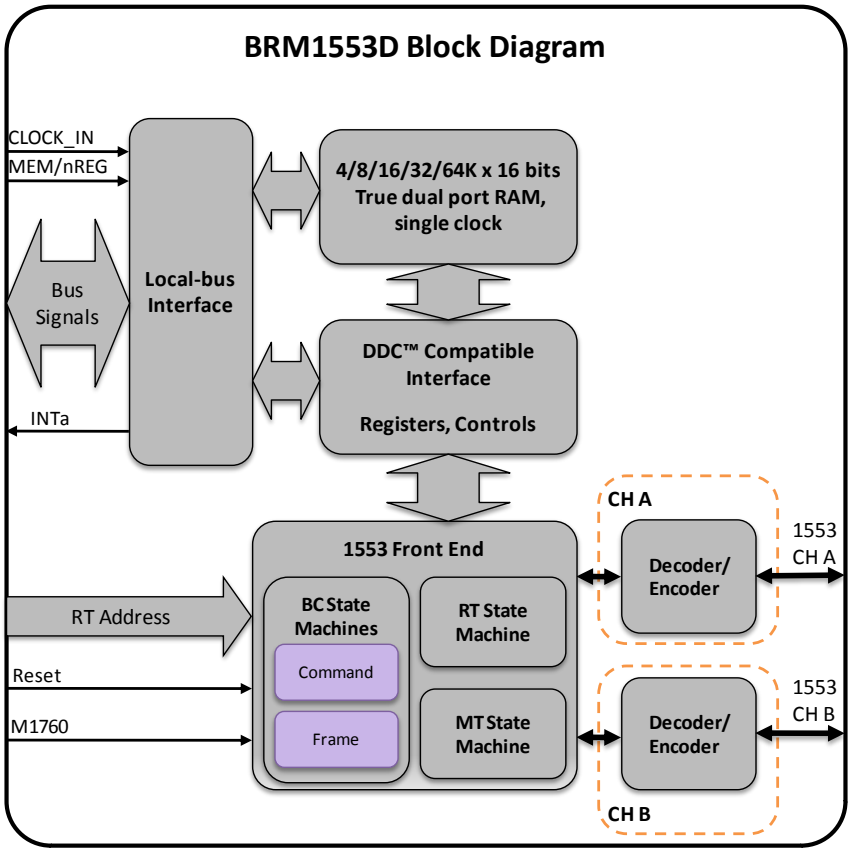
* BRM1553D was designed to support the subset of features used by most applications in order to provide a small gate count and cost-effective replacement.

BLOCK DIAGRAM

The BRM1553D Remote Terminal (RT) and Monitor (MT) mode core incorporates two decoders that translate the serial-bus messages from the MIL-STD-1553 Manchester coding and format into 16-bit parallel data accompanied by status indications for each word. Two concurrently-operated state machines, the RT state machine and the MT state machine, analyze these words.

The RT state machine identifies a set of these bus words as a valid message: transmit, receive, mode or broadcast message. When the RT state machine decides it has to store a word to or fetch a word from the subsystem, it asks the backend to interface with the internal memory array and store or fetch that word.

When transmitting words, a word is fetched from the host interface by the backend logic and is loaded into the encoder by the dual-channel RT state machine. The encoder formats the words into serial Manchester 2 coding and emits them to the 1553 transceivers and onto bus A or B.



The dual-channel Monitor state machine searches for valid commands. When it finds one, it checks if the command defines a message for monitoring. If so, the Monitor state machine manages the process of storing the words, one by one, in the interface memory at a predefined location.

The received and transmitted words are arranged in a dual-port memory according to the memory mapping of the enhanced mini-ACE remote terminal. The BRM1553D RT and MT MODE implements all memory modes of operations as described below.

The CPU controls the BRM1553D RT and MT MODE by programming the dual-port memory for message-specific settings and by programming a set of configuration registers for device-wide controls. A special select signal, MEM_nReg, selects between these two sections and is defined by the CPU for each read and write cycle.

The memory is a true, dual-port RAM as defined by the FPGA target with both sides independently reading or writing data. The CPU supplies the memory control signals, address, data, chip-select and write-enable synchronized with the clock signal supplied to the core. This synchronized approach ensures robustness of operation. Since the core and the user logic work with the same clock, the design has no transient effects.

The BRM1553D core was designed to work with any even-number Mhz larger than 12. The core was designed to work with the same clock that is used by the user logic that writes or reads memory and registers data. Thus, any read or write access to the core must be synchronous with the clock that is fed into the core, otherwise data inconsistency may occur. If an odd clock is used, say 55Mhz, it is important to use a PLL that will multiply the clock by two and this 110Mhz clock be fed to the core.

COMPATIBILITY

BRM1553D is fully compatible with MIL-STD-1553B Notice 2 at 1Mbps data-rate. The RT was validated according to test plan from MIL-HDBK-1553A.

On the 1553 bus side, the BRM1553D IP core can be connected to any transceiver-transformer pair or to the Sital Discrete Transceiver™ (see Sital Discrete Transceiver documentation for details). The transceiver should be selected in accordance with the supply voltage and bus requirements.

The IP core also supports the TX Inhibit line for both A and B channels.

On the backend side, the BRM1553D IP core is software compatible with DDC® MINI-ACE® or Enhanced MINI-ACE® interfaces.

FPGA REQUIREMENTS

FPGA Gate Count

Sital's BRM1553D requires very little space from FPGA even for complex applications. The following table shows examples of the area usage in various FPGA devices:

Vendor	Product Family	Area Usage (4-LUT count)	
		BC+RT+MT	RT Only
Altera	Stratix	4315	3250
	Cyclone	4320	3261
Xilinx	Virtex-II	4020	3066
	Spartan 3	4017	3063

- These numbers are approximate
- Other FPGA vendors and families are available
- Actual area usage may vary according to IP core configuration

FPGA Pads and Pins

The following pins are used from the FPGA:

- 10 pins to connect to transceiver (5 pins for each 1553 channel), or 14 pins (7 pins for each channel) – in case the Sital Discrete transceiver is used.
- One pin to connect to license key (if hardware key is selected for licensing; see Licensing Options for details).
- Optional 7 pins are used for RT address – in case external configuration of RT address is required.
- All pins are standard FPGA pads.

Memory

- Internal FPGA Dual-Port RAM of 2, 4, 8, 16, 32, 64K by 16 bits, depending on user's requirements for memory.

RAM

RAM is used as buffer for the transmitted or received data from the 1553 bus. The BRM1553D IP core supports any number of address lines. Each address is of 16 bits.

User should select the size of memory with accordance to FPGA limitations and project requirements.

This parameter is set once by Sital during the synthesis for the customer and cannot be changed by the customer during operation. See Ordering Information for details.

CLOCK

The BRM1553D IP core can work with any clock frequency of 12MHz and higher in steps of 2MHz. This ensures the reduction in clock domains in the application design. In most cases, user should select the clock frequency in accordance with the clock that drives the CPU or bus which connects to the IP core's backend.

This parameter is set once by Sital during the synthesis for the customer and cannot be changed by the customer during operation. See Ordering Information for details.

SUPPORTED FPGAS

The BRM1553D IP core can be used in most FPGA with sufficient number of LUTs and memory.

Currently the FPGA families from the following vendors are supported:

- Xilinx
- Actel
- Altera
- Lattice
- QuickLogic

For other FPGAs or ASICs, please consult Sital.

This parameter is set once by Sital during the synthesis for the customer and cannot be changed by the customer during operation. See Ordering Information for details.

BRM1553D DELIVERABLES

- EDIF Netlist of the core for the target FPGA technology, clock frequency and memory size
- Comprehensive user manual
- Top Test bench that instantiates all of these components to a working example including:
    - A Transceiver VHDL model that connects to the core with 2 buses
    - A bus tester VHDL model that generates 1553 messages and checks the return replies
- A simulation script for compiling and running the core

AVAILABLE CONFIGURATIONS

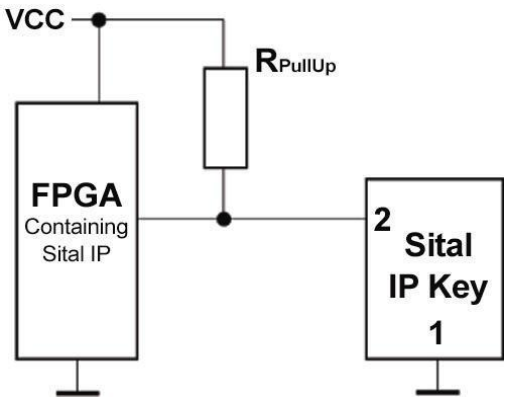
BRM1553D can serve as Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT) or any combination.

For IP Core setup, configuration and operation, see the BRM1553D User Guide.

BRM1553D HARDWARE KEY

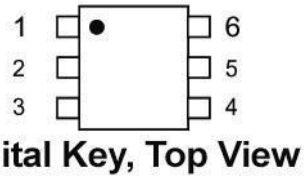
A Sital IP Security Key is required for operating Sital's IP Cores. The key uses a 6-pin small package (3.9mm x 4.3mm). One pin is connected to GND (Pin 1) and another pin (Pin 2) should be connected to the security pin at the FPGA. The security key is part of the IP core and the user must assign a bi-directional pin at the FPGA to support the key. This pin should also be connected to a pull-up resistor of 1K to 2.2K. All other pins (3, 4, 5 and 6) are not connected.

Operating Circuit



VCC supply in the range of 3V to 5.2V

Pin Configuraion



Sital Key, Top View

Pinout:
Pin 1 ---------- GND
Pin 2 ---------- IO
All other pins --- Not Connected

Hardware Key Electrical Characteristics

(T_A = -40°C to +85°C; see Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pullup Voltage	V_{PUP}		2.8		5.25	V
Pullup Resistance	R_{PUP}		1		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 2, 3)			1000	pF
Input Load Current	I_L	I/O pin at V_{PUP}	0.05		6.7	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 3, 4, 5)	0.5		V_{PUP} – 1.8	V
Input Low Voltage	V_{IL}	(Notes 6)			0.3	V
Low-to-High Switching Threshold	V_{TH}	(Notes 3, 4, 7)	1.0		V_{PUP} –1.0	V
Switching Hysteresis	V_{HY}	(Notes 3, 4, 8)	0.21		1.70	V
Output Low Voltage	V_{OL}	At 4mA (Note 9)			0.4	V
Data Retention (Notes 10, 11)	t_{DR}	At 85°C (worst case)	40			years

Note 1: Specifications at T_A = -40°C are guaranteed by design only and not production-tested.
Note 2: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied, the parasite capacitance will not affect normal communications.
Note 3: Guaranteed by design, characterization and/or simulation only. Not production tested.

Note 4: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is itself a function of V_{PUP}, R_{PUP}, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 5: Voltage below which, during a falling edge on IO, a logic 0 is detected.
Note 6: The voltage on IO needs to be less or equal to $V_{IL(MAX)}$ at all times the FPGA is driving IO to a logic-0 level.
Note 7: Voltage above which, during a rising edge on IO, a logic 1 is detected.
Note 8: After V_{TH} is crossed during a rising edge on IO, the voltage on IO has to drop by at least V_{HY} to be detected as logic '0'.
Note 9: The I-V characteristic is linear for voltages less than 1V.
Note 10: Data retention is degraded as T_A increases.
Note 11: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.

Hardware Key Absolute Maximum Ratings

I/O Voltage to GND	-0.5V, +6V
I/O Sink Current	20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Hardware Key Synthesis Procedure

The IP core EDIF net list embeds a single PAD for the signal “to_key” that connects to the external key. If you are synthesizing your design with a synthesizer and you are making the 1553 IP core a black box, your synthesizer will not know that a PAD is inside the black box and will embed a buffer for that pin. You must then issue a NOPAD command for that pin in your VHDL code. For every synthesizer this is unique. Please refer to its manual for instructions.

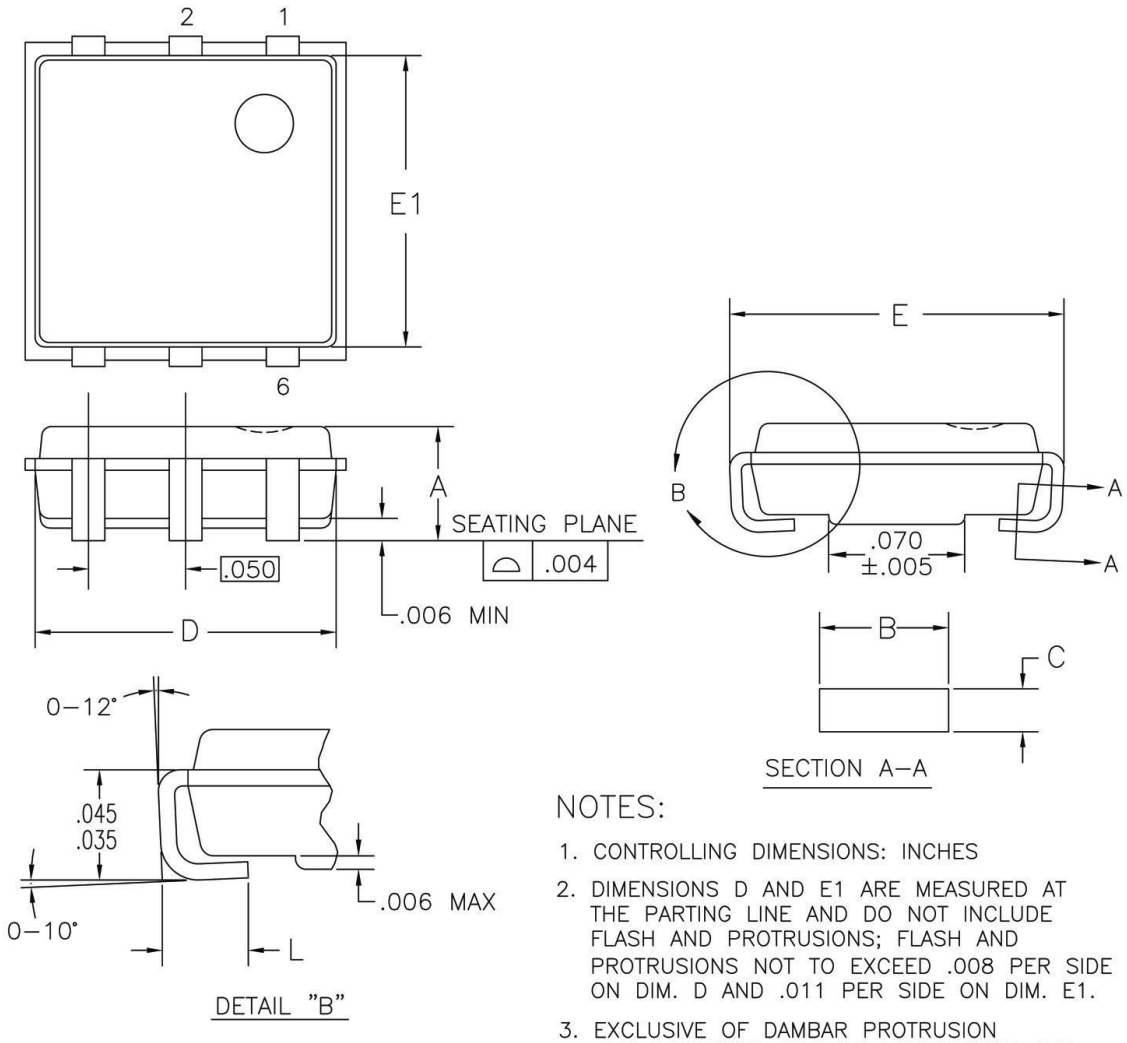
In Precision Synthesis, use the NOPAD attribute.

If your synthesizer reads your HDL code and the EDIF provided for the core, this operation is not required.

Hardware Key Ordering Information

Keys will be provided in accordance with the orders of BRM1553D. See Ordering Information for details.

Hardware Key Mechanical Drawings



NOTES:

1. CONTROLLING DIMENSIONS: INCHES
2. DIMENSIONS D AND E1 ARE MEASURED AT THE PARTING LINE AND DO NOT INCLUDE FLASH AND PROTRUSIONS; FLASH AND PROTRUSIONS NOT TO EXCEED .008 PER SIDE ON DIM. D AND .011 PER SIDE ON DIM. E1.
3. EXCLUSIVE OF DAMBAR PROTRUSION AND INTRUSION; DAMBAR PROTRUSION AND INTRUSION NOT TO BE POSITIONED ON FOOT OR LOWER RADIUS OF LEAD.

SYMBOL	DIMENSIONS INCHES			DIMENSIONS MILLIMMETERS			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	.051	.055	.059	1.295	1.397	1.499	
B	.016	.017	.019	0.406	0.432	0.483	3
C	.005	.006	.008	0.127	0.152	0.203	
D	.153	.155	.157	3.886	3.937	3.988	2
E	.163	.169	.175	4.140	4.293	4.445	
E1	.144	.150	.152	3.658	3.810	3.861	2
L	.025	.032	.039	0.635	0.813	0.991	

ORDERING INFORMATION

Part Number (*) Optional parameters (**)

BRM1553D-BCRTMT-S-KP-ALxxx-16-66

Part Number	Clock Frequency (Optional)
12 200	Number represents clock frequency in MHz. Any even number between 12 and 200 is available.

Part Number	Memory Configuration (Optional)
4	4K x 16 bits
8	8K x 16 bits
16	16K x 16 bits
32	32K x 16 bits
64	64K x 16 bits

Part Number	FPGA Selection (Optional)
AL	Altera
XL	Xilinx
LT	Lattice
AC	Actel
QL	QuickLogic
xxx	Indicate FPGA Family or part number

Part Number	Licensing Option
KP	Hardware Key, Lead-Free

Part Number	Transceiver Option
S	Sital Discrete Transceiver
T	Any Other Transceiver

Part Number	IP Core Type
BC	Bus Controller
RT	Remote Terminal
MT	Monitor Terminal
RTMT	Remote Terminal & Monitor Terminal
BCRTMT	Bus Controller, Remote Terminal & Monitor

(*) Part Number must include IP Core Type, Transceiver Option and Licensing Option
(**) FPGA Selection, Memory Configuration and Clock Frequency are optional parameters

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